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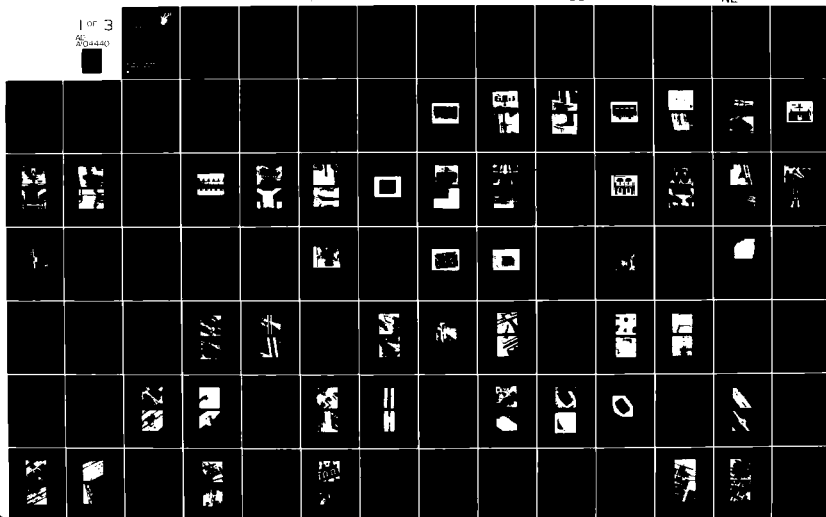
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Final Technical Report
July 1981

FAILURE MECHANISM STUDY OF GaAs TECHNOLOGY

Hughes Aircraft Company

**Dr. L.S. Bowman
W. Tarn**

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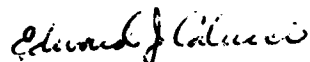
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) In this report we have discussed the characterization of the power FETs procured for this program and failure analysis of low noise devices, including wire bonding failures and environmental stress test failures. A method of etching gold while leaving the underlying refractory metals relatively unaffected was explained. An analysis of the Type A-6 low noise FET was given, in which a failure mode was discussed that involved possible channel doping compensation. Results were then presented on device (over)		

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failures from high and medium temperature stress tests on low noise FETs.

A number of medium power devices were received from RADC for analysis. These were packaged FETs that had been subjected to various stresses at Texas Instruments on a RADC/TI reliability contract. Typically, the devices had failed during deliberate stressing to the maximum electrical limits or in temperature stress tests.

Failure mechanism studies of two different ohmic contact metallizations showed that both fabrication procedures produced reliable contacts. Constant elevated temperature tests of gold-based gate diode FETs from two different manufacturers showed that one device type was considerably less prone to gate diode failure than the other, indicating the necessity of additional work on the gold gate versus aluminum gate reliability question.

Failures were investigated that involve problems associated with gold contact pads overlaying aluminum gate pads with a refractory metal interface. Finally, temperature-accelerated studies of the resistance of aluminum gates were carried out.

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EVALUATION

The intent of this contractual program was to investigate the physics of failure mechanisms associated with gallium arsenide (GaAs) metal epitaxial semiconductor field-effect transistors (MESFETs). Failed devices of both power and small signal types evolving from two independently sponsored reliability contracts, (1) "Reliability Evaluation of GaAs FETs" Contract number F30606-79-C-0037, which investigated the reliability of power GaAs FETs and (2) "Reliability Investigation of Low Noise GaAs FETs," Contract number F30602-78-C-0295, which investigated the reliability of small signal devices, were to be analyzed and provide the basis for more detailed studies. Further in-depth failure analysis must be performed in order to establish failure modes and mechanisms in GaAs FET devices. Since this study did not fully meet its original goals, the reader is cautioned that the data resulting from this program may have limitations.

Edward J. Calucci
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Project Engineer

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From the inception of the proposal writing through the first nineteen months of work on this contract, Glenn O. Ladd was Program Manager. Lawrence S. Bowman became Program Manager in May 1980 when Dr. Ladd transferred to another division of Hughes Aircraft Company. The authors gratefully acknowledge Dr. Ladd's many contributions to the successful completion of this program.

We acknowledge the many contributions of B. Bernor, D. Higgins, W. Klatskin, and G. Williams, who worked on the program, and the continual support of Dr. T. A. Midford, Manager of the Hughes Torrance Research Center. We have greatly appreciated the interest and encouragement of E. J. Calucci and J. Carroll of the Rome Air Development Center in accomplishing the program goals.

TABLE OF CONTENTS

<u>Section</u>		<u>Page</u>
1.0	INTRODUCTION	1
2.0	FET CHARACTERIZATION	3
2.1	Characterization Details	3
2.2	Summary	29
3.0	FAILURE ANALYSIS OF LOW NOISE DEVICES	31
3.1	RADC/Hughes Low Noise GaAs FET Reliability Program	31
3.2	Wire Bonding Failures	31
3.3	Environmental Stress Test Failures	37
3.4	Gold Etch Using Ga	41
3.5	Type A-6 Low Noise FET	42
	3.5.1 Background	42
	3.5.2 Failure Analysis	44
3.6	Selected High Temperature Stress Failures	54
	3.6.1 Type A-10 FET	54
	3.6.2 Type D-1 FET	60
	3.6.3 Type H-1 FET	60
	3.6.4 Type H-11 FET	67
	3.6.5 Type N-3 FET	69
3.7	Medium Temperature Stress Test Failures	72
4.0	FAILURE ANALYSIS OF MEDIUM POWER DEVICES	77
4.1	RADC/TI Medium Power GaAs FET Reliability Program	77
4.2	Maximum Electrical Limits	77
	4.2.1 Example: Type T-500/8 FET vs Tests	79
	4.2.2 Comparison of Failures vs. Test Method	84
	4.2.3 Summary Comments	90
4.3	Temperature Stress Test	96
	4.3.1 Type M-400/6 FETs	96
	4.3.2 Type D-250/6 FETs	104
5.0	FAILURE MECHANISM STUDIES	115
5.1	Ohmic Contact Tests	115
5.2	Gold Gate Reliability	117
5.3	Gold-Aluminum Connectors	121
5.4	Resistance of Gold Pad - Aluminum Gate Transition	132

TABLE OF CONTENTS (CONTINUED)

<u>Section</u>	<u>Page</u>
6.0 . SUMMARY	137
7.0 REFERENCES	139
<u>Appendix</u>	
A RECENT RESULTS OF FAILURE ANALYSIS OBTAINED AFTER PREPARATION OF THE FINAL REPORT DRAFT	141

LIST OF ILLUSTRATIONS

<u>Figure</u>		<u>Page</u>
2-1	Optical photograph of FET D-60/8.	7
2-2	FET D-60/8. (a) SEM photograph, overall view, 168 X. (b) Gate connector, showing glass missing in some areas.	8
2-3	FET D-60/8. (a) Gate finger end at 4700X. Glass adhered only to ohmic contacts. (b) Au-refractory layer is 2600A thick.	9
2-4	Optical photograph of FET D-250/6.	10
2-5	FET D-250/6. (a) Overall view. (b) Gate end, showing ragged gate edge and good step coverage.	11
2-6	FET D-250/6. (a) Gate connector at 4500X. Note very smooth ohmic contact metal surface and edge. (b) Gate end at 18000X.	12
2-7	Optical photograph of FET F-600/8.	13
2-8	FET F-600/8 (a) Overall, 170X (b) Gate connector, glass intact.	14
2-9	FET F-600/8. (a) Gate electrode, glass intact, showing etched Al and recessed channel. 9000X. (b) Gate over source, 4500X, glass removed.	15
2-10	Optical photograph of FET F-1000/12.	17
2-11	FET F-1000/12 at 84X (a) and 1900X (b) with glass coating for 2nd level metal isolation intact.	18
2-12	F-1000/12. (a) End of gate finger with glass in place. Note recessed area on left (source pad). (b) Glass removed.	19
2-13	Optical photograph of FET N-200/6.	20
2-14	FET N-200/6. (a) Overall view, 107X. (b) Gate connector area, glass intact.	21
2-15	FET N-200/6. (a) Gate finger end, with glass, 9000X. (b) Glass removed, 4800X.	22
2-16	Optical photograph of FET N-250/11.	24
2-17	FET N-250/11. (a) Overall view. (b) View of gate area with glass.	25

LIST OF ILLUSTRATIONS (Continued)

<u>Figure</u>		<u>Page</u>
2-18	FET N-250/11. (a) Gate with glass, gate length is 1.2 μm . (b) After glass removal.	26
2-19	(a) Packaged FET P-200/5. (b) Packaged FET T-500/8.	27
2-20	Packaged FET D-800/6.	28
3-1	Type N-2, showing lifting of overlay metal during gold wire bonding.	33
3-2	Type P-5 chip, showing smeared wire bonds required to obtain adhesion.	35
3-3	Type R-5 chip, showing gross test probe defects which resulted in wire bonding problems.	36
3-4	Type R-51, showing failure of source bond wires.	38
3-5	Type R-51, #1, which failed during the random vibration test. (a) SEM photograph of fractured die, 600X. (b) Sketch identifying areas of interest.	40
3-6	Type A-6, No. 1, prior to temperature stressing.	45
3-7	Type A-6, No. 1, prior to temperature stressing.	46
3-8	(a and b) Type A-6, No. 140, after 533 hours at 260°C, 4V, 10 mA.	48
3-8	(c) Type A-6, No. 140, after 533 hours at 260°C, 4V, 10 mA.	49
3-9	Type A-6, No. 135, after 533 hours at 260°C, 4V, 10 mA. (a) Detail of gate connector. (b) Detail of gate finger end.	50
3-10	Type A-6, No. 137, after 533 hours at 260°C, 4V, 10 mA. Gold removed. (a) Overall view. (b) Detail of gate connector region.	52
3-11	Type A-6, No. 137, after 533 hours at 260°C, 4V, 10 mA. Gold removed. (a) Mesa edge, showing alloyed contact residue. (b) Gate detail.	53
3-12	SEM photographs of the failed Type A-10, No. 162 FET.	58

LIST OF ILLUSTRATIONS (Continued)

<u>Figure</u>		<u>Page</u>
3-13	Type A-10, No. 162 FET. SEM/EDAX mappings. (a) Aluminum; (b) Gold.	59
3-14	SEM photographs of the failed Type D-1, No. 100 FET.	61
3-15	Type D-1, No. 100 FET. (a) SEM photograph of a portion of the gate stripe showing discoloration; (b) EDAX gold mapping of the same area.	62
3-16	(a) SEM photograph of failed Type H-1, No. 44 FET at 102X. (b) Close-up view of the gate pad to gate transition region, showing pitted aluminum and gold-aluminum intermetallic compound.	64
3-17	(a) Type H-1, No. 44 FET. Gold gate pad and aluminum transition at 250X. (b) Aluminum mapping of the failed Type H-1, No. 44 FET.	65
3-17	(c) Gold mapping of the failed Type H-1, No. 44 FET.	66
3-18	Type H-1, No. 44 FET. (a) 2000X view of the gate short failure site in Figure 3-16(a); (b) Gold mapping, showing gold migration from the source and drain metallizations to the gate region.	68
3-19	(a) SEM photograph of the failed Type H-11, No. 183 FET at 150X; (b) 6000X view of the gate failure site.	70
3-20	Type H-11, No. 183 FET. (a) SEM photograph at 2500X of the gate pad to gate stripe transition showing metallization voids and nodules; (b) 6000X photograph of the upper left corner of the drain contact pad in Fig. 3-19 (a).	71
3-21	(a) SEM photograph of failed Type N-3, No. 8 FET at 160X. (b) Nodules on the gate stripe.	73
3-22	(a) SEM photograph of failed Type N-32, No. 38 FET at 390X; (b) Close-up view of the left gate pad transition showing the gold-aluminum intermetallic compound formation involving source, gate, and drain metallizations.	75
4-1	Type T-500/8, #1, after maximum V_{DS} , $V_G = 0$; electrical stress test.	82
4-2	Type T-500/8, #2, after maximum V_{DS} , $V_G = 0$; electrical stress test.	83

LIST OF ILLUSTRATIONS (Continued)

<u>Figure</u>		<u>Page</u>
4-3	Type D-250/6, FET from Test A. (a) 200X, note cracked die. (b) 4000X, note black spots.	85
4-4	Type D-250/6 FET, from Test B. (a) 200X, showing burned gate wire. (b) Gate burnout.	87
4-5	Type M-400/6, #3, from Test B.	88
4-6	(a) Type T-500/8, #11, at 1000X. (b) Type D-250/6, #14, at 2000X.	89
4-7	Type D-250/6, #22, from Test D. (a) 400X, showing location of burn-out in mid-finger. (b) 4000X, showing lifted gate and replica in passivating glass.	91
4-8	Type N-250/11-P, #25, Test D, 200X. (b) Type T-500/8, #4, Test D, 1000X.	92
4-9	Type M-400/6, #11, Test D. (a) Optical photograph (color original) at 500X. (b) SEM photograph.	93
4-10	(a) Type M-400/6, #10, Test E, 1000X. (b) Type D-250/6, #21, Test E, 400X.	94
4-11	Type N-250/11-P, #9, Test E. (a) 400X. (b) 1000X.	95
4-12	SEM photographs of the Type M-400/6 12J device.	98
4-13	SEM photographs of the Type M-400/6 device.	100
4-14	SEM photographs of the Type M-400/6 14J device.	101
4-15	SEM photographs of new Type M-400/6 FET. (a) Overall view at 195X; (b) Gate pad to gate finger transition at 7800X.	102
4-16	SEM photographs of the Type D-250/6 #16 FET. (a) Overall view at 100X; (b) Gate pad to gate finger transition at 5040X.	106
4-17	SEM photographs of the Type D-250/6 #26 FET. (a) Overall view at 120X; (b) Detail of catastrophic failure showing involvement of source, drain, and gate (270X).	107
4-18	SEM photographs of Type D-250/6 #29 FET. (a) Bubble in glass passivation layer (8400X); (b) Piece missing from glass passivation layer (8940X).	109

LIST OF ILLUSTRATIONS (Continued)

<u>Figure</u>		<u>Page</u>
4-19	SEM photographs of the Type D-250/6 #37 device.	110
4-20	SEM photographs of the Type D-250/6 #44 device.	111
4-21	SEM photographs of the Type D-250/6 #45 device.	112
5-1	Change of ohmic contact resistance upon heating for thick Au-Ge/Ni ohmic contact alloyed at 480°C.	118
5-2	Change of ohmic contact resistance upon heating for thin Au-Ge/Ni ohmic contact alloyed at approximately 360°C.	119
5-3	Gate connector designs, gold-aluminum. (a) Gold overlays Al in band area. (b) Gold does not overlay Al in band area.	122
5-4	Type H-1 FET, sample A. (a) After 40/42g wedge force. (b) After 312 hours storage at 260°C.	126
5-5	Type H-1, sample B. (a) Initial appearance, 500X. (b) After 312 hours at 260°C. 500X magnification.	127
5-6	Type H-1 FET, sample B, after 576 hours at 260°C in N ₂ gas. (a) Optical photograph at 600X; (b) SEM photograph at 500X.	128
5-7	Type H-1 FET, sample C. (a) After 20/22g normal wedge force. (b) After 312 hours at 260°C.	129
5-8	Type H-1 FET, sample D. (a) After 20/22g wedge force at right pad edge. (b) After 312 hours at 260°C.	130
5-9	Type H-1 FET, sample E. (a) As received condition. (b) After 312 hours at 260°C.	131
5-10	FET type E-10 bonded for gate-to-gate resistance tests.	134
5-11	Current at 50 mV through a 0.5 μ m gate stripe heated without bias as 200°C and 260°C.	135

LIST OF TABLES

<u>Table</u>		<u>Page</u>
2-1	GaAs FETs for Failure Mechanism Study	4
2-2	Manufacturer's Published Specifications	5
3-1	Summary of Mounting Defects	32
3-2	Failure Rates of Type A-6 FET vs. Type 78-A-2 FET	43
3-3	Manufacturer's Specifications	55
3-4	Important Physical Characteristics of Low Noise FET Chips	56
4-1	RADC-Furnished Power FETs Evaluated	78
4-2	Summary of Device Failure Modes, T-500/8	80
4-3	Failure Mode Detail, T-500/8	81
4-4	Characteristics of Failed Type M-400/6 Devices Received From RADC	97
4-5	Characteristics of Failed Type D-250/6 Devices Received From RADC	105
5-1	Ohmic Contact Process Parameters	116
5-2	Gate Diode Degradation at 260°C, Type T-1000/10 FET	120
5-3	Type H-1 FET: Unbiased Device Storage at 260°C	125

1.0 INTRODUCTION

This is the final report covering Hughes Aircraft Company's work during the period from 31 August 1978 through 31 August 1980 on Rome Air Development Center Contract No. F30602-78-C-0326. The objective of this program is to establish the physics of failure, physical limitations and maximum stresses of gallium arsenide (GaAs) metal-epitaxial-semiconductor field effect transistors (MESFETs). The devices studied included small signal and power devices from both domestic and foreign markets. Failure mechanisms that were studied include electromigration, ohmic contact degradation, Schottky contact degradation, doping defects, metal deplating, and passivation defects. Not only was the device itself evaluated, but also assembly methods and packaging, such as wire bond integrity, connections, compatible material, protective coatings, and packaging seals.

In addition to the study of specific failure mechanisms, a task has been carried out on failure analysis of FETs from other contracts being supported by the Rome Air Development Center (RADC). Devices were supplied to this program from two RADC programs, "Reliability of Low Noise GaAs FETs" with Hughes⁽¹⁾ and "Reliability Investigation of GaAs Power FETs" with Texas Instruments⁽²⁾. In the final report for the RADC/Hughes program device failures were characterized, wherever possible, by mean times to failure, and the activation energy was obtained.⁽¹⁾

In this report we have combined information derived from the failure mechanism studies with results of various analytical methods to determine the causes of device failures.

2.0 FET CHARACTERIZATION

Our approach to the procurement of FETs for this program was to concentrate on power GaAs FETs. This approach was taken because Hughes is also the contractor for the RADC program on low noise FET reliability.⁽¹⁾ From that program we expected to obtain sufficient low noise FETs for failure analysis, without having to use contract funds to obtain them for the purposes of the present program. The devices that were procured for this program are listed in Table 2-1. The type code number consists of a letter designation as well as two numbers separated by a slash mark. The first number is the nominal output power of the device in milliwatts, and the second number is the operating frequency in GHz. The table shows the distribution of FETs between chips and packaged devices. It also shows the assignment of FETs to various tests during the program. "ENVIR" refers to four devices that were placed on environmental tests early in the program. The "SEM/EDAX" column refers to those devices that were committed to evaluation in the scanning electron microscope (SEM) with EDAX capability. The "REMAIN" column refers to those devices that are available for further testing.

Our approach to the characterization of the FETs was first to photograph them optically and then to do a thorough evaluation in the scanning electron microscope, using the EDAX feature as needed. For a complete characterization, the devices should also have been probed for their DC characteristics and mounted and tested in an RF circuit. This work was not done because of the small number of devices of each type that we could afford to purchase. For reference, the manufacturer's published specifications are given in Table 2-2.

2.1 CHARACTERIZATION DETAILS

This section is devoted to a discussion of the results of the optical microscope and scanning electron microscope/EDAX examinations. Table 2-2 gives the manufacturer's published specifications for each device.

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TABLE 2-1
GaAs FETs FOR FAILURE MECHANISM STUDY

Type Code	Procured		Disposition		
	Chip	Pkg	Envir	SEM/EDAX	Remain
D-60/8	3	--	--	--	3
D-250/6	3	--	--	1	2
D-800/6	--	2	1	--	1
F-600/4	--	2	--	--	2
F-600/8	3	--	--	1	2
F-500/12	--	2	--	--	2
F-1000/12	2	--	--	1	1
M-400/6	--	2	--	1	1
N-200/6	3	--	--	1	2
N-600/7	--	2	--	--	2
N-250/11	3	--	--	1	2
P-200/5	--	2	1	--	1
T-500/8	--	3	2	--	1
Totals	17	15	4	6	22

TABLE 2-2
MANUFACTURER'S PUBLISHED SPECIFICATIONS

Type Code	D-60/8	D-250/6	D-800/6	F-600/4	F-600/8	F-500/12	F-1000/12	M-400/6	N-300/6	N-600/7	N-250/11	P-200/5	T-500/8
<u>TYP. PARA.</u> f, CHz	8	6	6	4	8	12	12	6	6	7.2	11	5	8
P _{out} , mW, at	65 ¹	250 ¹	800 ¹	630 ¹	562 ¹	500 ¹	1100 ¹	400	300 ¹	630	130	200	500
G, dB	10	9	5.5	9	6	7	5.5	6.5	7.0	5.9	7.0	6	4
I _{DS} , mA	0.5I _{DSS}	150	450	190	175	0.5I _{DSS}	750	-	-	275	80	70	~150
V _{DS} , V	8	7	8	10	10	10	10	9	7	9	9	8	-
I _{DSS} , mA at	120	320	900	380	350	650	1500	300	400	800	220	130	300
V _{DS} , V	3	4	4	5	5	5	5	5	4	4	4	5	5
g _m , mmho, at	34	105	150	90	90	150	300	75	90	130	40	40	-
I _{DS} , mA/V _{DS} , V	~80/5	~300/5	~750/5	160/5	160/5	300/5	700/5	-/5	100/3	250/3	50/3	130/5	-
V _P , V at	-3	-6	-6	-4	-4	-	-	-6	-4.5	-5.5	-5.5	6	3.6
I _{DS} , mA/V _{DS} , V	1/3	2/3	5/3	10/3	10/3	-	-	-/5	1/3	20/3	5/3	0.5/5	~150/5
θ _J , °C/W	70	40	25	50	50	30	17	35	55	30	100	-	75
<u>MAX. RATING</u> V _{DS} , V/I _{DS} , mA	10/60	10/160	10/450	15/190	15/-	12/-	12/-	10/-	10/-	20/-	20/-	12/-	10/-
V _{GS} , V				-5	-5	-5	-5	-5	-10	-12	-12	-8	-5
I _{CS} , mA	150	300	600	-	-	-	-	-	-	-	-	-	-
P _{DISS} , W	0.8	2.5	5.0	3.0	3.0	5.0	8.8	3.2	2.5	5.0	1.5	1.4	2.13
T _{ch} , °C	175	175	175	175	175	175	175	150	175	175	175	-	185

Note 1. Power out at 1 dB gain compression.

D-60/8 (Figures 2-1, 2-2, and 2-3)

This FET has two symmetrically placed gate pads feeding the linear gate stripe. The gate metallization was accomplished by the liftoff process. The gate is offset toward the source side. The ends of the gate stripe turn at 90° as they cross the mesa edge. The glass passivation is not totally present over the gate region.

D-250/6 (Figures 2-4, 2-5, and 2-6)

This device is an eight-fingered medium power FET. The gate metallization, which was obviously accomplished by a lift process, has somewhat ragged edges. The gate is offset toward the source, and the gate metallization is slightly undercut, perhaps by a slight etch of the underlying refractory layer after lifting. The thickness of the gate metallization appears to be less than half the gate length. The gate connector crosses a shallow, sloping mesa step. The EDAX scan shows that the overlay glass contains silicon.

F-600/8 (Figures 2-7, 2-8, and 2-9)

This is a medium power FET, where the gate metallization is connected by an overlay over the source metallization. SEM photographs of the gate prior to the removal of the glass show a ragged gate profile with the top narrower than the bottom. This indicates that the gate was etched rather than lifted. There is some evidence of recessing of the gate electrode. The EDAX scans show only GaAs, aluminum and gold. One EDAX scan does show germanium in the source-drain metallization area, indicating that the ohmic contact is probably gold-germanium. The separation between the gate and source metallization in the overlay area appears to be small. The step coverage is not particularly good, as well, indicating some sites for separation of the gate metallization where it crossed over the source. The mesa on this device shows two etching steps, as have been previously reported for the F-type process. There is little or no evidence of profiling of the channel in this power FET, in contrast to some reports made earlier by vendors F and N. On this device we looked at the SEM photographs to determine which metallization crossed over. On the F-1000/12 device the SEM photographs with the glass attached showed very clearly a difference in contrast between the gate and the source over-crossing metallization. In

E2253

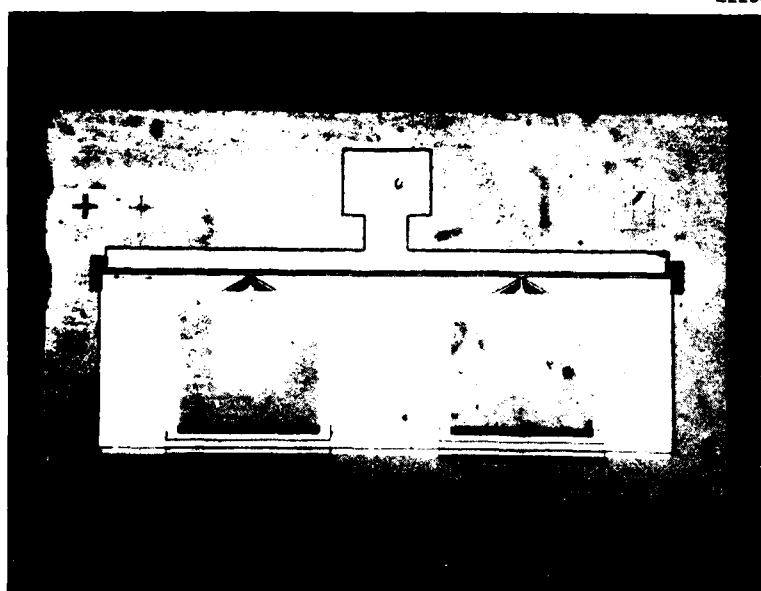
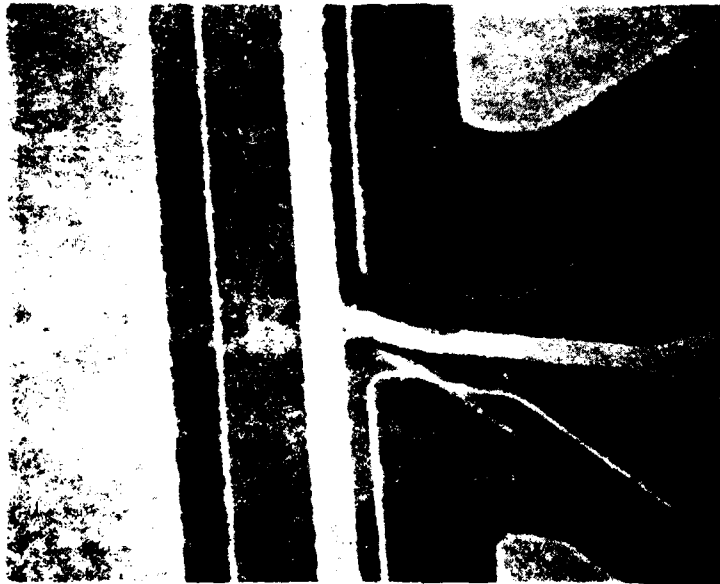


Figure 2-1 Optical photograph of FET D-60/8.

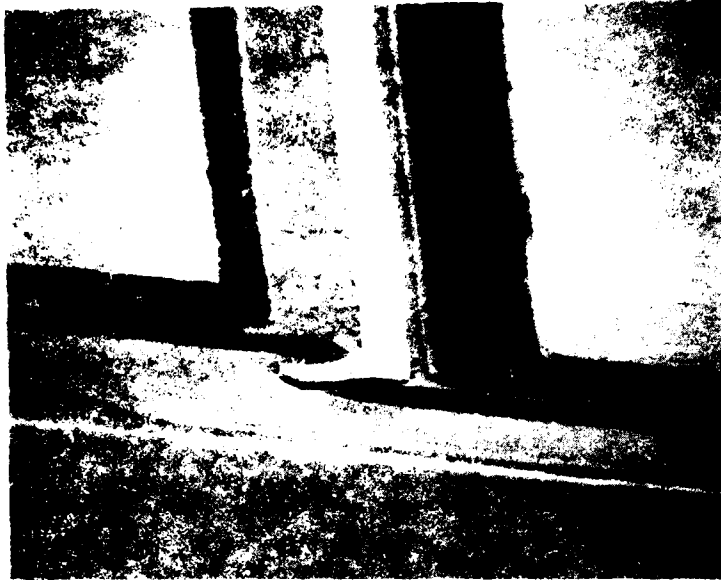


(a)



(b)

Figure 2-2 FET D-60/8. (a) SEM photograph, overall view, 168 X. (b) Gate connector, showing glass missing in some areas. S-D spacing is 4.7 μm . 4500X mag.



(a)



(b)

Figure 2-3 FFT D-60/8. (a) Gate finger end at 4700X. Glass adhered only to ohmic contacts. (b) Au-retractory layer is 2600Å thick. Note slight undercut of metal, etched channel, fringe due to lift-off. Gate length is 1.3 μm .

E2252

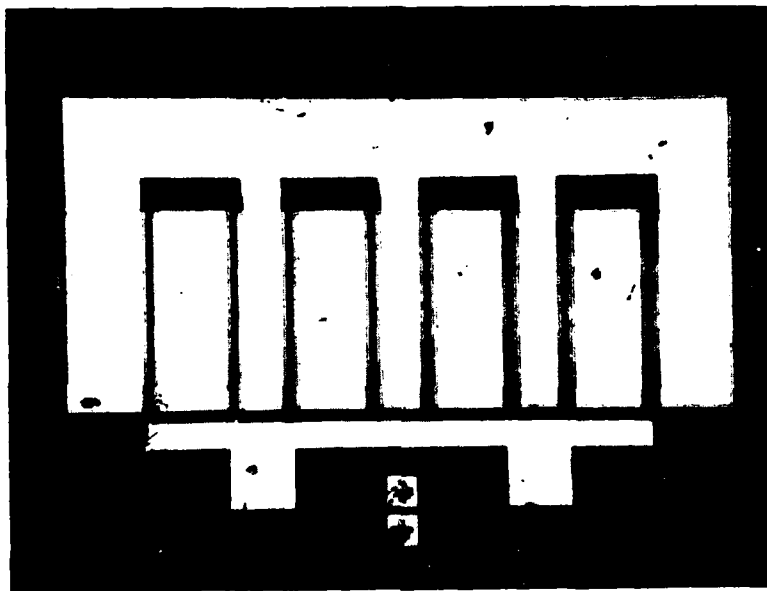
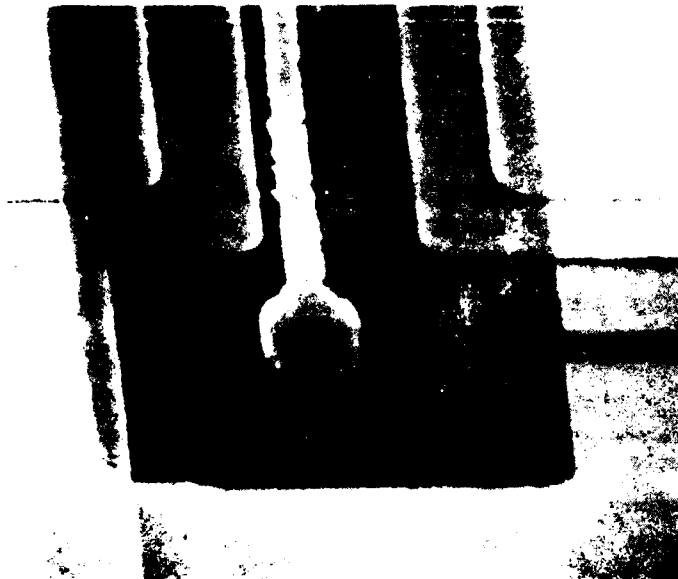


Figure 2-4 Optical photograph of FET D-250/6.

E2733



(a)



(b)

Figure 2-5 FET D-250/6. (a) Overall view. (b) Gate end, showing ragged gate edge and good step coverage.

E2734



(a)



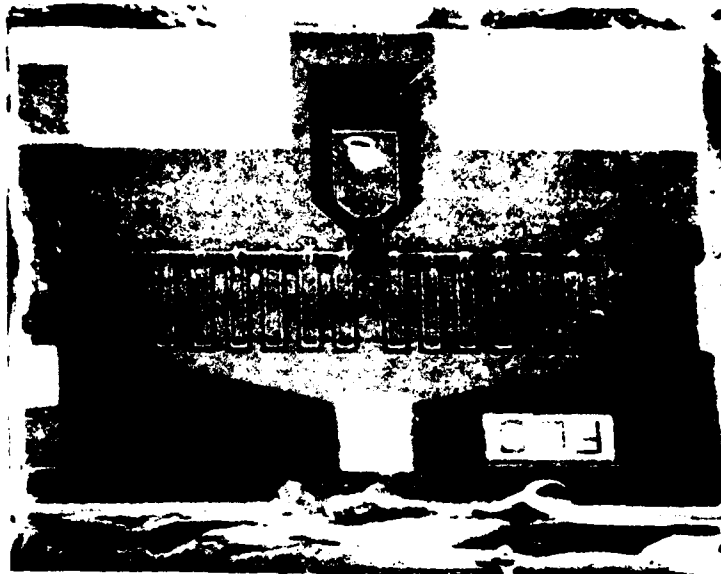
(b)

Figure 2.6 FET D-250/6. (a) Gate connector at 4500X. Note very smooth ohmic contact metal surface and edge. (b) Gate end at 18000X. Apparent gate metal thickness is 2800 Å. Note ragged edge.

E2256



Figure 2-7 Optical photograph of FET F-600/8.



(a)



(b)

Figure 2-8 FET F-600/8 (a) Overall, 170X (b) Gate connector, glass intact. Note ragged gate, poor separation of gate overlay from source by thin glass. Gate is aluminum.

E2736



(a)



(b)

Figure 2-9 FET F-600/8. (a) Gate electrode, glass intact, showing etched Al and recessed channel. 9000X. (b) Gate over source, 4500X, glass removed. Note poor step coverage.

the F-1000/12 device the protective glass apparently was used as the separating layer between the two metallizations. In this F-600/8 device, it is apparent that a different process was used.

F-1000/12 (Figures 2-10, 2-11, and 2-12)

This is a medium power FET, and the SEM photographs, prior to removal of the glass, show a clean gate profile. After removal of the glass using buffered HF, the gate lines were severely eroded. On this device the source metallization overlays the gate metallization, and the source metal connectors have good step coverage over the gate. If these gates were made by the lift process, they have a very clean profile. There is a possibility that they may have been etched or cleaned up after lifting.

The EDAX scans did not reveal anything other than gold/aluminum/GaAs, so there is no conclusion as to the composition of the contact metallization. The source metallization connectors are quite grainy.

N-200/6 (Figures 2-13, 2-14, and 2-15)

This is a six-gate medium power FET. The gate metallization is aluminum. The gate is connected to a gold pad using a titanium/platinum connector. In this device, no gold actually overlays the aluminum, according to the EDAX scans.

In the scans with the glass applied, the gate appears to be relatively well defined. After removal of the glass, the aluminum did not suffer any tremendous damage; in fact, it looked somewhat similar to the aluminum prior to removal of the glass. The gate is not particularly well defined, has somewhat ragged edges, and is located in the center of the channel. The mesa step on this device is perhaps twice the thickness of the gate metallization, and the gate metallization shows a number of voids and incipient cracks where it crosses the mesa step, though there is a possibility that these were caused by the HF etch.

The contact metallization does not show any nickel or germanium, but the overlay appears to be titanium/platinum/gold, according to the EDAX scans.

E2257

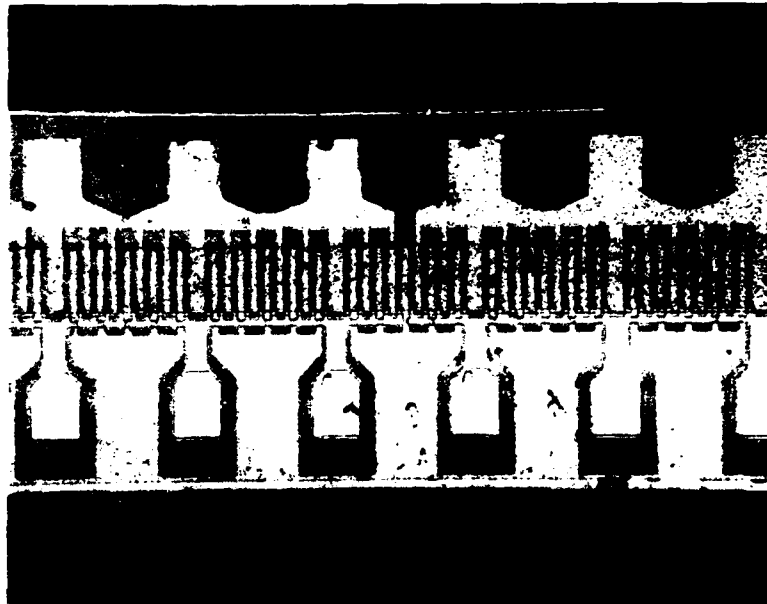
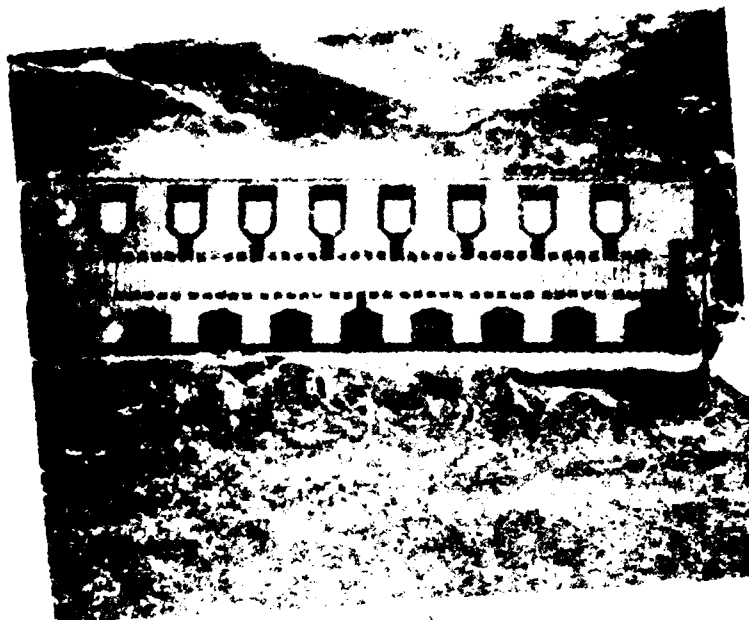


Figure 2-10 Optical photograph of FET F-1000/12.



E2739



(a)



(b)

Figure 2-12 F-1000/12. (a) End of gate finger with glass in place. Note recessed area on left (source pad). (b) Glass removed. Note good isolation of upper source lead from lower gate metal.

E2248

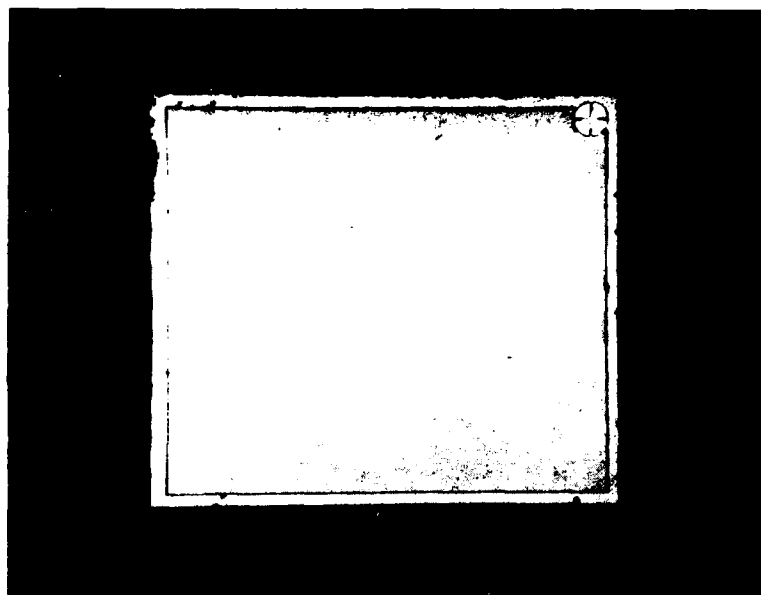
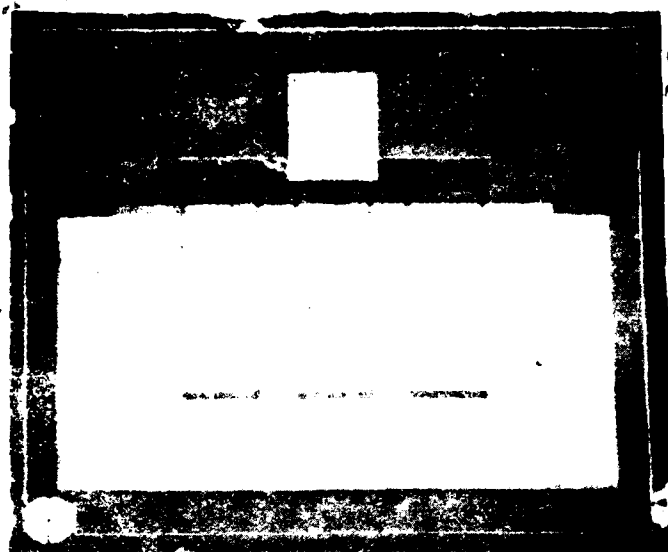
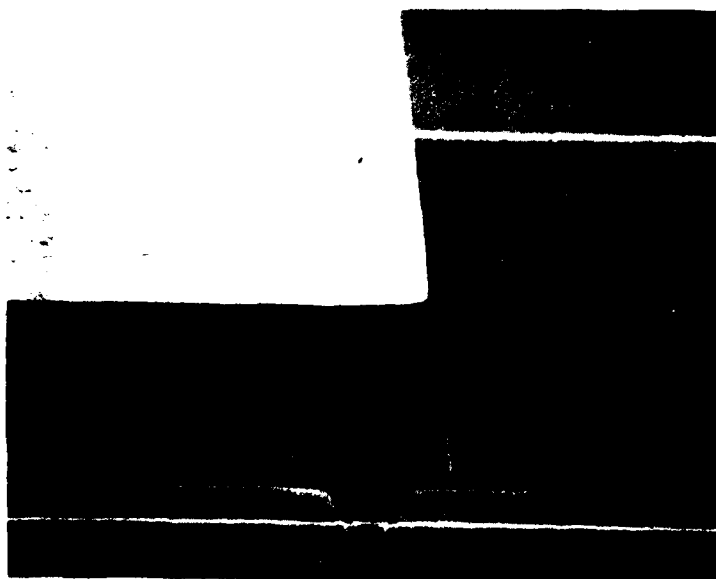


Figure 2-13 Optical photograph of FET N-200/6.

E2740



(a)



(b)

Figure 2-14 FET N-200/6. (a) Overall view, 107X.
(b) Gate connector area, glass intact.

E2741



(a)



(b)

Figure 2-15 FET N-200/6. (a) Gate finger end, with glass, 9000X. (b) Glass removed, 4800X. Gate length prior to glass etch was $1.0\text{ }\mu\text{m}$, S-D spacing $3.45\text{ }\mu\text{m}$. Note slight GaAs etch around S-D metal, sharp mesa step and height compared to Al gate thickness.

There is no clear evidence for etching of the GaAs prior to deposition of the gate metallization. However, the GaAs was etched prior to deposition of the ohmic contact. Probably, this transistor was made using the self-aligned technology which vendor N has developed, and there is no opportunity in that process for etching of the channel.

N-250/11 (Figures 2-16, 2-17, and 2-18).

This device shows a technology similar to that of vendor F and apparently is carried out with a separately aligned gate and an etched-down channel. The channel topography shows that the channel was etched probably twice, once in the vicinity of the contact and again just underneath the gate electrode in a manner similar to what has been reported previously by vendor N. However, the etch under the gate appears to be shallow, perhaps 500\AA , and this shallowness may not be intentional. In this device the source connector clearly overlays the gate metallization. In contrast to most of the other devices, the alloyed ohmic contact shows a dark and light grain structure in the SEM photographs. The scan of the ohmic contact shows chromium and nickel in addition to gold. N type devices of a few years ago used Au-Ge/Pt. Platinum appears to have been superseded by chromium and nickel, perhaps nichrome. Chromium shows up more strongly in the scan of the ohmic contact metal, but is of course not seen in the scan of the heavy gold overlay metallization.

The scans of the gate transition show chromium, an equal percentage of platinum, and a trace of titanium. However, the gold pad directly overlays the aluminum gate electrode, and it is also apparent that the aluminum gate electrode has been etched prior to deposition of the gold overlay. In this device it is the overlay metallization for the source and drain that appears to have been electroplated. The source overlays across the gate metallization appear to be well separated and covered by heavy gold metallization, so that there is little chance for defects to develop at the crossover steps.

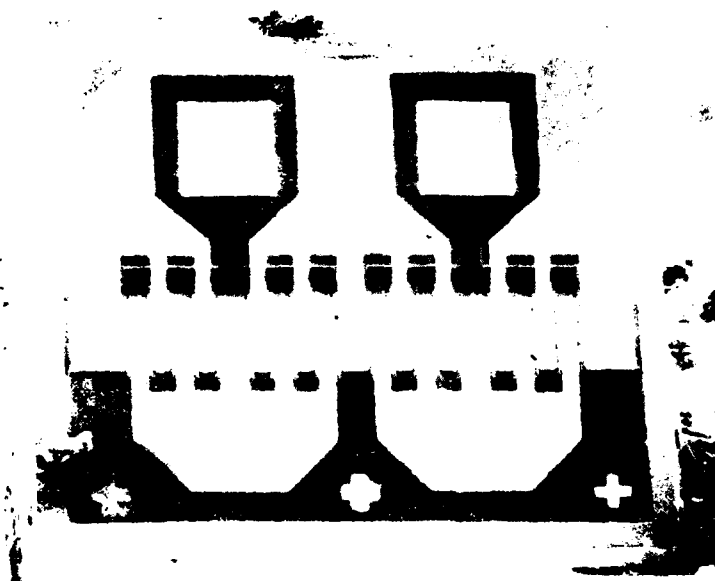
Packaging

Standard microstrip packages and carriers were used for the packaged FETs. Figures 2-19 and 2-20 show photographs of the package exteriors.

E2249



Figure 2-16 Optical photograph of FET N-250/11.



(a)



(b)

Figure 2-17 FET N-250/11. (a) Overall view. (b) View of gate area with glass. Source crosses over gate. Note gate transition to bond pad at top.

E2743

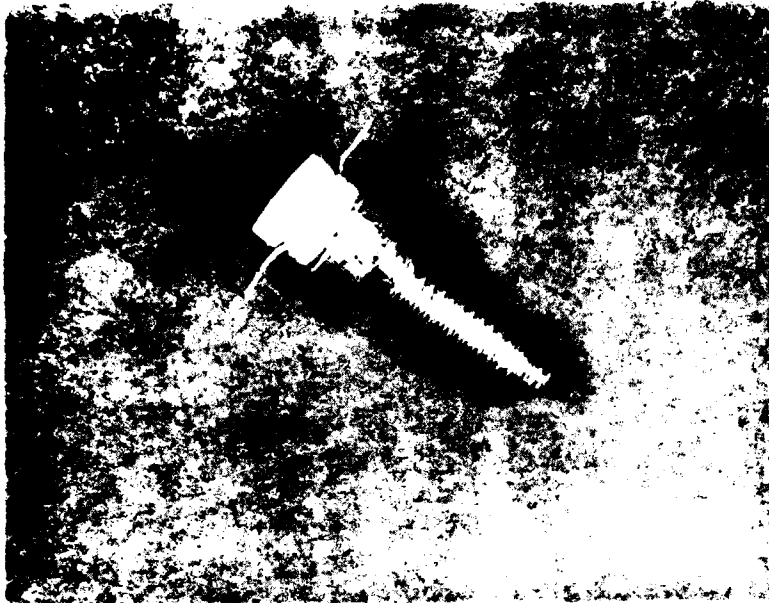


(a)

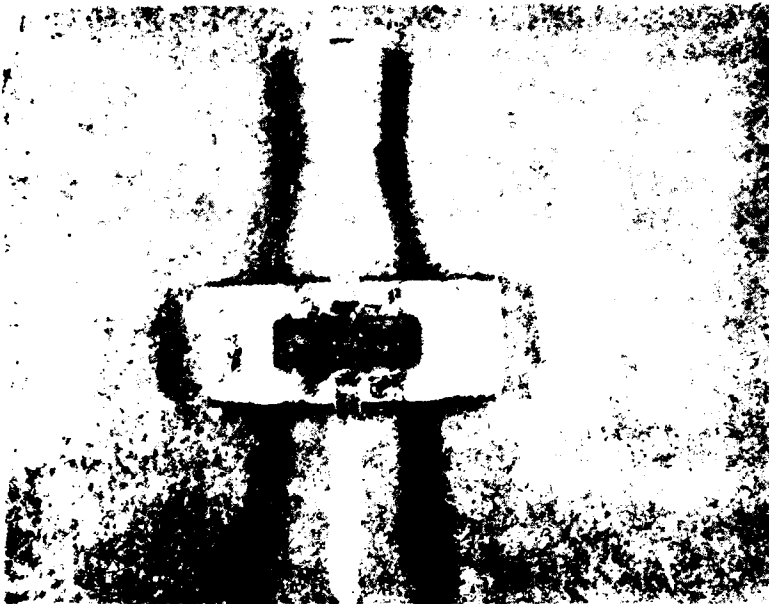


(b)

Figure 2-18 FET N-250/11. (a) Gate with glass, gate length is 1.2 μm . (b) After glass removal. Note: Source contact is (intentionally?) aligned close to etched channel, nearly overlapping edge. Gate appears not to be intentionally etched into channel.



(a)



(b)

Figure 2-19 (a) Packaged FET P-200/5
(b) Packaged FET T-500/8.

E2745

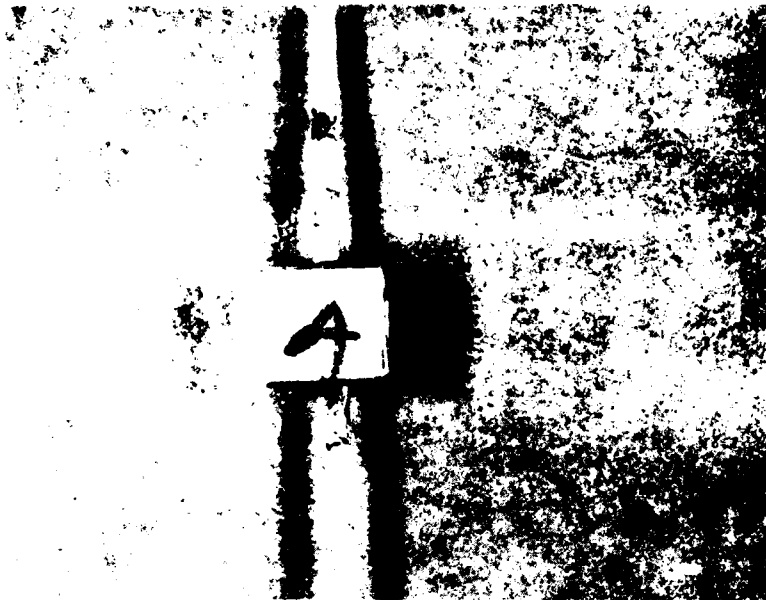


Figure 2-20 Packaged FET D-800/6.

2.2 SUMMARY

The optical and SEM examinations were relatively successful with respect to determining the method of fabrication and the materials of fabrication. Most manufacturers use the gold-germanium ohmic contact. Because of the mass ratios, it is relatively difficult to measure germanium in the presence of gallium and arsenic. The germanium peak falls directly between the gallium and arsenic peaks. Fortunately, this determination is probably not as interesting as the determination of the refractory overlay metal which is frequently used in the contact process. We found evidence of nickel, platinum, and chromium, where we refer now to characterizations which were also carried out on low noise FETs on the RADC/Hughes Low Noise GaAs FET Reliability contract.⁽¹⁾ One might expect some differences in the reliability and electromigration properties of these ohmic contacts, depending on the overlay metal and construction that was used. We carried out some tests on ohmic contacts on this program, which are discussed in Section 5.1.

The alignment accuracy and edge definition achieved by most of the manufacturer's processes are quite good. A common defect is the appearance of a ragged edge on the metallization resulting from slight failure of the lift-off process. This type of defect may be serious in power FETs that use second level metallizations to interconnect the source and/or gate contacts. When these ragged metal edges are allowed to occur, the glass that is put over the first layer metal may be penetrated by these metal spikes when the second level metallization approach was used. The two metal layers could thus become short-circuited.

The constitution of the various glass overlays was not determined in most cases, except that silicon was measured in one case. Except for one D-type device, the glass layer appeared to adhere relatively well.

One problem is the determination of the exact composition of the gate diode. Hughes has found in previous reliability testing programs that adequate thickness of the refractory metal layers under the gold in gold-based gate electrode systems is important to achieve high reliability. When these metal layers are too thin it is assumed that the gate diode becomes nonrectifying because of the penetration of the

refractory metal layers by the upper layer of gold. As will be shown in Section 3.4, we have developed a method for removing the gold without disturbing either the GaAs surface or the refractory metals, which remain underneath the gold. This method allows us to obtain accurate characterizations of the refractory metallizations.

3.0 FAILURE ANALYSIS OF LOW NOISE DEVICES

3.1 RADC/HUGHES LOW NOISE GaAs FET RELIABILITY PROGRAM

One purpose of the RADC/Hughes Low Noise FET Reliability Program is to determine the failure rates and failure mechanisms of FETs subjected to various environmental and elevated temperature stresses. Devices from that program were delivered to this program for in-depth failure analysis. Details of results on the Reliability Program are given in the Final Report.⁽¹⁾ This section reports results of the failure analysis on devices from that program.

3.2 WIRE BONDING FAILURES

We have collected data on the problems associated with wire bonding of the FETs. In the usual sense this would not be considered an operational failure, but the problems encountered reveal something about device quality. The defects observed may be present to a lesser degree, even in well-screened devices. In other words, they are characteristic of the device processing.

Table 3-1 gives a summary of some of the problems encountered. On the Type H-1 FET we found the devices breaking up readily during wire bonding. This problem could be the result of a flaw in the wire or die bonding procedures, but we think not because our people have mounted hundreds of other FETs using the same equipment, die and wire bonding processes, and carrier. Occasionally, we do encounter GaAs substrates which appear to be unusually brittle, usually manifest by a high incidence of wafer cracking during lapping and polishing. Or, the excessive breaking up of the Type H-1 FETs might be a result of the dicing process, which sometimes requires bending or rolling of the wafer after scribing to get cleavage. In any event, we feel that this incident is potentially significant to device reliability and should be noted.

Two instances of metal lifting occurred during wire bonding. The Type N-2 devices, Figure 3-1, showed lifting of the ohmic contact overlay metal (Au), and the Type A-1 devices exhibited peeling of the gate pad. SEM examination of Type A-1 FETs positively confirmed that the pad had separated from the GaAs, leaving a visible mark, but without any pulling away of the GaAs.

TABLE 3-1
SUMMARY OF MOUNTING DEFECTS

Device*	Losses	Comments
A-1	22 of 50	Au gate bond pad lifted at wire bonding, high percentage of peeling leaves 28 balance suspect.
H-1	9 of 45	Mounting personnel found they broke up at mounting.
N-2	5 of 9	Gold overlay lifted during wire bonding.
P-5	5 of 10	No gold overlay. Bonding technique required: "Smear and Lift Away." This produced tenuous bonds.
R-5	3 of 7	Gross test artifacts made bonding difficult.

*For characterization data, see final report for Contract No. F30602-78-C-0295, "Reliability Investigation of Low Noise FETs". (1)

E2473

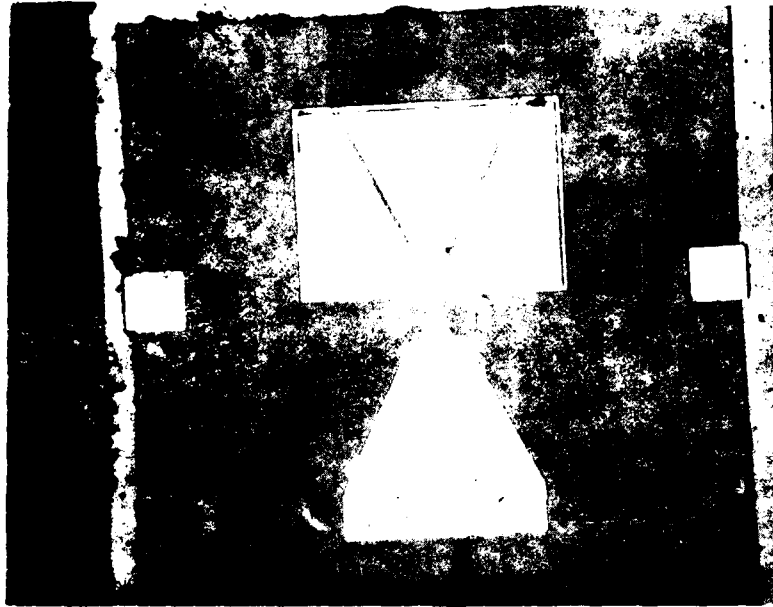


Figure 3-1 Type N-2, showing lifting of overlay metal during gold wire bonding.

The lifting problem was characteristic of the FETs from these two types of devices that we had purchased, and we were therefore unable to use the units in our tests. This situation usually indicates an adhesion problem between the device metallization and the GaAs or underlying metal. If the metal adheres well, either the GaAs is pulled out of the surface or the wire breaks during pulling. In none of the cases here was the wire pulled other than in the normal bonding cycle.

The manufacturer of Type A-1 FETs was contacted regarding the metallization peeling problem. He was well aware of the difficulties and had already improved his manufacturing process. He sent us 50 replacement units at no charge. We have experienced no metal adherence problems with the improved devices, designated Type A-6, and in fact the metallization appears to be of superior quality. More discussion of Type A-6 FETs given in Section 3.5.

In the case of the Type N-2 FETs, information received from the vendor indicates that he supplies FETs in four reliability grades, and that we had purchased the industrial (lowest) grade. With this grade device peeling is allowed with ultrasonic bonding if the pull force is greater than 4 grams. In our procedure, gold wire bonding with 0.7 mil diameter wire is carried out at a temperature of 230°C using a cold wedge and slight ultrasonic scrubbing. We are unable to conclude, therefore, that the devices themselves were faulty, and in retrospect we might have earlier requested reject samples from the vendor for bonding evaluation.

To check further on the manufacturer's metallization process and wire bonding procedures, we delidded a packaged Type N-21 device and examined the Type N-2 FET chip inside. The wire bonds were well placed, nicely formed, and showed good adherence. Our recommendations, therefore, are to buy devices having the reliability grade suitable to the application, to evaluate incoming chips for bond pull strength, and strictly to follow the manufacturer's procedures for wire bonding.

The Type P-5 device metallization was thin and hard. The bonding operator had to smear the gold wire to achieve a bond, Figure 3-2. In our experience this situation indicates low bond strength, but we did not pull test any of the bonds.

On the Type R devices, fairly gross test probe marks were observed, as shown in Figure 3-3. The metallization is so badly gouged that bonding was quite difficult.

E2474

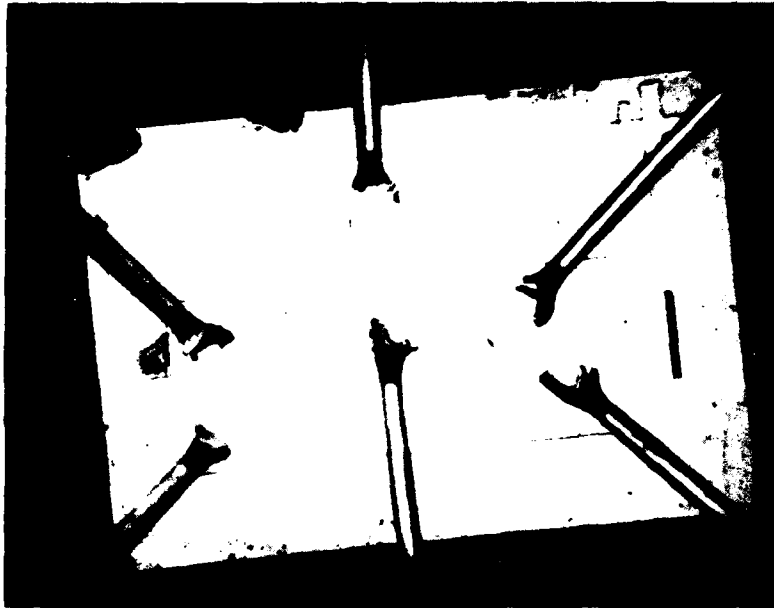


Figure 3-2 Type P-5 chip, showing smeared wire bonds required to obtain adhesion.

E2476

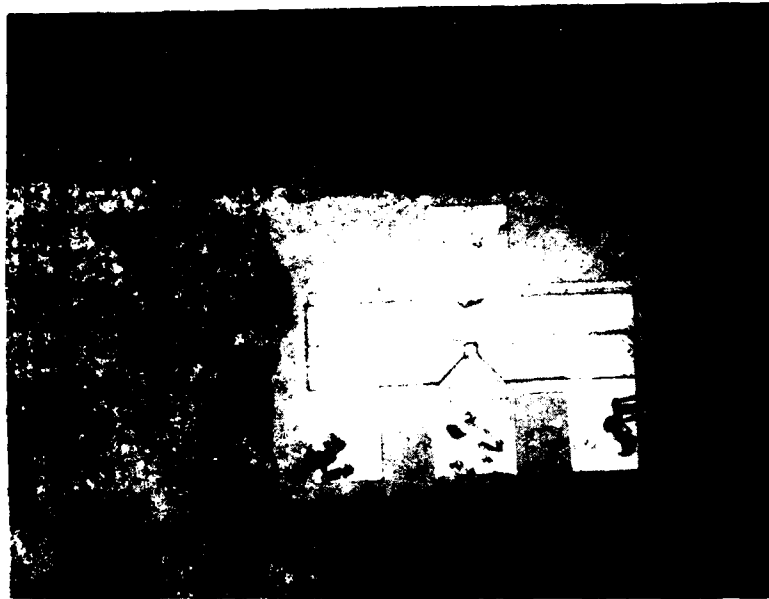


Figure 3-3 Type R-5 chip, showing gross test probe defects which resulted in wire bonding problems.

Although these judgments are subjective, they indicate a low level of quality control in many of the devices that were purchased. However, the devices used in the Low Noise GaAs FET Reliability Program were obtained from lots manufactured two to three years ago, and the results reported here may not be truly representative of results of similar tests, were they to be performed on FETs obtained from the manufacturer's current inventory.

In every instance where we contacted a manufacturer concerning possible problems with his FETs, he was already aware of the situation and was wholly responsive to our inquiry in helping us to resolve the difficulties. Our recommendation is to purchase devices from the latest lots and to contact the supplier immediately if any questions arise concerning his products. To eliminate most bonding problems, pull tests should be done on a routine basis for every wafer batch. The user can also ask for the manufacturer's certification of screening of the wafer lot for bonding defects and then buy only from that lot.

3.3 ENVIRONMENTAL STRESS TEST FAILURES

Two Type R-51 FETs failed during environmental stress testing. Figure 3-4 shows the interior of a Type R-51 FET that failed slightly the hermeticity test after random vibration. When the unit was delidded, no gross reason for the hermeticity failure was found. However, we did discover a reliability problem. This was the alloying of the gold-tin eutectic die bonding material with the source bond wires. The brittle character of the Au-Sn alloy on the wire, as well as the resulting necked-down Au wire shown near the bottom of the photograph, caused us to list this unit as an incipient failure.

Judging from the character of the alloying, we doubt that the alloying could have occurred during wire bonding. Wire bonding temperatures were usually not high enough to result in that much alloying. This is a subjective judgment, however, and is conditioned by the belief that the vendor would have rejected such a part in the pre-cap visual inspection.

A more likely cause of the alloying is overheating during sealing of the cap, which was also done using gold-tin. The obvious solution to this problem is to limit the amount of

E2746



Figure 3-4 Type R-51, showing failure of source bond wires.

eutectic material used during die bonding. Also, the source wires should not be bonded to the area wetted by the eutectic.

This sort of incipient failure indicates that high reliability parts should be delidded as part of the qualification process to assure that the die bond is properly formed and that proper source bond lead dress is achieved.

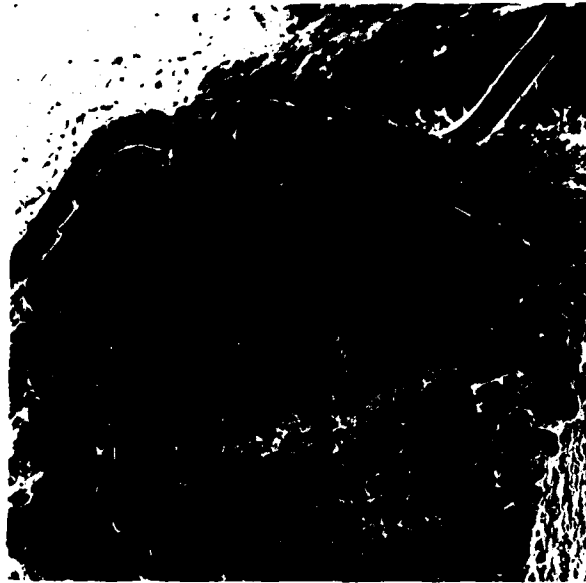
One other Type R-51 FET from the Low Noise GaAs FET Reliability Program failed catastrophically by drain-source short after random vibration during the environmental stress testing sequence. It had slightly failed the initial hermeticity test, but was retained in the testing sequence. It was a Type R-51, our Device Number 1.

The failed device was opened and examined. We found that the FET die had cracked approximately in half. One portion was still attached to the header, and one piece was held in the package by the drain wire. In the failure the drain wire apparently short circuited to a source wire or ground.

Figure 3-5 shows a SEM photograph and sketch of the piece of die which remained attached to the header. Prolonged examination of the package by SEM and optical microscope failed to reveal any evidence of GaAs on the header surface from which the other piece of the die had become detached. We concluded that the die had fractured during the random vibration test, which consisted of successive stages at 15g, 45g, and 60g along one axis. In this case the axis was perpendicular to the die mounting surface.

We hypothesize that the die was not completely wetted to the header solder and likely was cantilevered on one edge, the edge which is still attached. The test vibration probably caused the fracture. For the population of all devices tested, this represents 1 failure in 15. It should also be noted that both R-51 devices failed the hermeticity test following the random vibration test. The fractured die failure is probably due to a quality control problem in die attach rather than indicating anything fundamental with regard to the GaAs FET. On the other hand, one might observe that, because of the more brittle nature of GaAs, the FETs may be less tolerant of insecure die mounting than silicon dice would be.

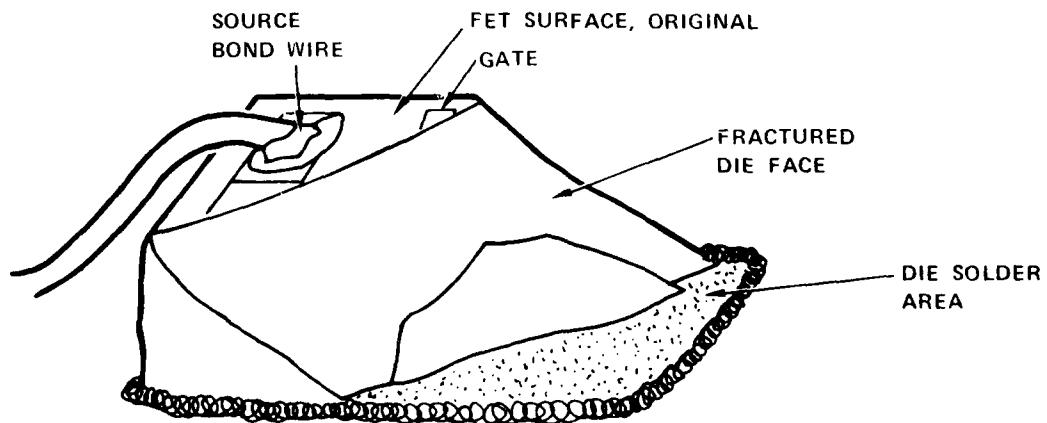
E2614



LNX 835

200X 60°

(a)



(b)

Figure 3-5 Type R-51, #1, which failed during the random vibration test. (a) SEM photograph of fractured die, 600X. (b) Sketch identifying areas of interest.

As a result of these tests, we recommend that packaged low noise FETs, and especially medium power FETs, be subjected to 100% vibration screening tests for any critical application, such as military or satellite use. Medium power FETs should be especially vulnerable because of the large die areas. However, no medium power FETs failed due to environmental testing on this program.

3.4 GOLD ETCH USING Ga

We have developed and applied what appears to be a previously unpublished technique for analyzing failed devices. The process allows us to preferentially strip the gold metallization from the device, leaving the refractory metal layers substantially undisturbed. An EDAX analysis of these layers can then be obtained, which otherwise would not have been possible.

The process is simple and can easily be done without special equipment. The steps are as follows:

1. Mount device on a glass slide using Apiezon W wax. Leave the area to be etched clean.
2. Fill a 50 ml beaker with liquid gallium to sufficient depth that the mounted device can be immersed in it. The gallium probably should be about 3-9's pure or better. We usually use 6-9's purity because it is procured in quantity for other purposes.
3. Heat the Ga to between 60°C and 80°C, using a Hg lab thermometer to measure the temperature. During heating, cover the Ga with DI water to a depth of about 1 cm.
4. When the temperature is stabilized, add concentrated HCl acid to the beaker, a drop at a time, until the Ga surface is clean and bright.
5. Immerse the FET into the Ga for about 3-5 minutes.

6. Inspect the device to determine if the gold is removed. The Ga dissolves the gold if the device has been wetted by the Ga. To assure wetting, the device must be clean prior to immersion.
7. Continue immersion until the desired amount of gold is removed. Periodically add drops of HCl to the water, if the Ga surface oxidizes. Note that the device must be immersed in the Ga. Dilute HCl will etch some metals, and even GaAs with prolonged immersion. Therefore, keep the device in the Ga, and upon removal rinse it with DI water.

Using this technique, we have successfully removed all the gold from failed FETs. An example is discussed in Section 3.5.

3.5 TYPE A-6 LOW NOISE FET

3.5.1 Background

The Type A-6 chip was tested at 220°C, 240°C, and 260°C in separate constant stress life tests on the Reliability of Low Noise GaAs FETs Program. The drain current changed much faster than we had predicted, based on typical failure rates of other vendor's FETs. The data are repeated in Table 3-2 and are compared with data on a Type 78-A-2 aluminum gate FET. Clearly the failure rates are much higher.

The DC characteristics of the FETs after testing were normal except that the g_m , I_{DSS} , V_p , and I_{DS} had all decreased dramatically. The gate breakdown voltage had increased, and the gate reverse current had decreased. The curve tracer display of the common drain characteristic was normal in shape, but with the lower current levels.

Our initial conclusion was that the channel doping had somehow decreased dramatically. Such a change in channel doping would be a new failure mode for us. We have never encountered this kind of failure on any other vendor's low noise or medium power FET. The comment refers to experience not only at Hughes Research Laboratories and Torrance Research Center, but also at the Hughes systems groups.

TABLE 3-2
FAILURE RATES OF TYPE A-6 FET
vs.
TYPE 78-A-2 FET

Temp., °C	Hours	Type A-6 ΔI_{DS} , %	Type 78-A-2 ΔI_{DS} , %
216°C	1200		Approx. -5
220°C	1223	-43	
231°C	1200		Approx. -15
240°C	1277	-79	
245°C	1000		Approx. -8
260°C	533	-77	

*Type 78A-2 is a 1 μ m (aluminum) gate FET. Data are from
"Reliability Study of GaAs FET," Final Report, RADC Contract
F30602-76-C-0374, June 1978, p. 54.(3)

We contacted Vendor A and asked them to trace the lot which they had sent us and tell us if they had experienced any difficulties. From this and subsequent conversations the following picture emerged.

Vendor A has been screening FET wafers in a high temperature test. Sample FETs are held under bias at 275°C. Good devices fail in 150 hours, poor ones in 30 hours or less. The failure criterion is a 1 dB change in $|S_{21}|^2$ at about 10 GHz. This criterion should correspond fairly closely to the RF failure criterion on a previous RADC/Hughes contract, which is a 1 dB change in associated gain with minimum noise figure tuning at 10 GHz.⁽³⁾

Vendor A told us that they have seen the problem both with VPE wafers and with ion implanted channels using bulk-grown substrates for the implant. Their tentative conclusion is that the substrates are contaminated. They have measured the gate capacitance during the heating cycle. The decrease of the capacitance with time confirms that the channel doping is decreasing, probably due to compensation from some fast-diffusing impurity.

3.5.2 Failure Analysis

We have carefully examined the topology of virgin and temperature-stressed Type A-6 FETs. We have also stripped the gold from one life-tested FET and have analyzed the gate metal. This work is reported below.

Figures 3-6 and 3-7 show Type A-6, No. 1, which has not been subjected to temperature stressing. In Figure 3-6, note the residue on the GaAs surface and the stains on the source/drain metallization. Close examination of Figure 3-7 shows that the residue also occurs in the channel area, but what looks like a GaAs surface in Figure 3-7 (a) is, in fact, the ohmic contact metal surface.

The Vendor A process makes use of gold plating to increase the thickness of the electrode metallizations and reduce parasitic resistance. As we will show below, the actual gate length of this "0.5 μm " gate FET is actually 0.8 μm . The high performance of this type FET is in large part due to the low gate resistance.



(a)



(b)

Figure 3-6 Type A-6, No. 1, prior to temperature stressing. Drain is on the left.

E2635



(a)



(b)

Figure 3-7 Type A-6, No. 1, prior to temperature stressing. Note plated-up gate electrode in center of photographs.

To build up the gate metal, it is first necessary to deposit Ti-W alloy. Then the gold is electroplated until it partially climbs over the photoresist edge. This procedure accounts for the peculiar "lifted edge" appearance of the edges of the metallization.

Figure 3-8 shows Type A-6, No. 140, after heating under a bias of $V_{DS} = 4$ V, $I_{DS} = 10$ mA for 533 hours at 260°C. The large asperity is a dust particle. Note the gold hillocks or grains growing out of the source and drain metal. They do not appear to grow on the gate metal, so they may be initiated by the ohmic contact. Figure 3-8(c) is especially interesting, because it indicates a foreign substance underneath the gate electrode edge on the drain side, which bridges the gap between the gate and drain ohmic contact metal. Although some surface contamination could have resulted from handling at Hughes, the foreign material we looked for would have been a residue of the manufacturer's fabrication process. The substance may be a residue of the material used to define the gate. In all likelihood this foreign substance is not photoresist. It may be the same material that appears as a residue on the rest of the die surface. We did not find as much of the residue on the other A-6 FETs we examined.

We should note that this residue could be a source of the impurity responsible for the failure. The possibility is discussed in more detail below.

Figure 3-9 shows Type A-6, No. 135, also heated for 533 hours at 260°C and biased at 4 V, 10 mA. On this FET we took a large number of SEM pictures and examined the channel area very carefully. The residue we saw on A-6, No. 140, was present, it appeared, but in very small amounts. Figure 3-9(b) shows that the ohmic contact metal lies just under the raised edge of the gate. Therefore, it is difficult to get a good view of the GaAs surface in the channel. The square "window" just above the gate connector in Figure 3-9(a) exposes the GaAs, but in this area the GaAs surface has been removed by the mesa etch. By careful examination, however, we confirmed that slight amounts of the residue were present. The amount on the die surface surrounding the FET metallization seems to be a good guide as to the amount to be found in the channel.

The final analysis involved using the gallium etch discussed in Section 3.4 for removal of the gold from one device after temperature stressing in order to examine better the gate and ohmic contact edges in the channel. The results are shown in

E2696



(a)



(b)

Figure 3-8 (a and b) Type A-6, No. 140, after 533 hours at 260°C, 4 V, 10 mA. Large asperity at top is debris, not part of FET.



(c)

Figure 3-8 (c) Type A-6, No. 140, after 533 hours at 260°C, 4 V, 10 mA. Note gold hillocks on source and drain electrodes and foreign substance between gate and drain metals.

E2638



(a)



(b)

Figure 3-9 Type A-6, No. 135, after 533 hours at 260°C, 4 V, 10 mA. (a) Detail of gate connector. (b) Detail of gate finger end.

Figures 3-10 and 3-11, where Type A-6, No. 137, heated 533 hours at 260°C under bias, is shown.

Figure 3-10(a) shows an overall view. The bright area on the gate pad is the residue of the gold bond wire, as are the other bright areas. Figure 3-10(b) shows the gate pad connector area. The gold has been completely removed from the gate metal proper, which was verified to be Ti-W.

Figure 3-11 shows two magnifications of the end of the gate finger. Figure 3-11(a) shows the irregularities in the gate edge, the width of the actual channel, and the residue of the ohmic contact. It also strongly suggests that the gate is recessed into the GaAs. This recession would tend to preclude etching of the gate metal edges as a definition process.

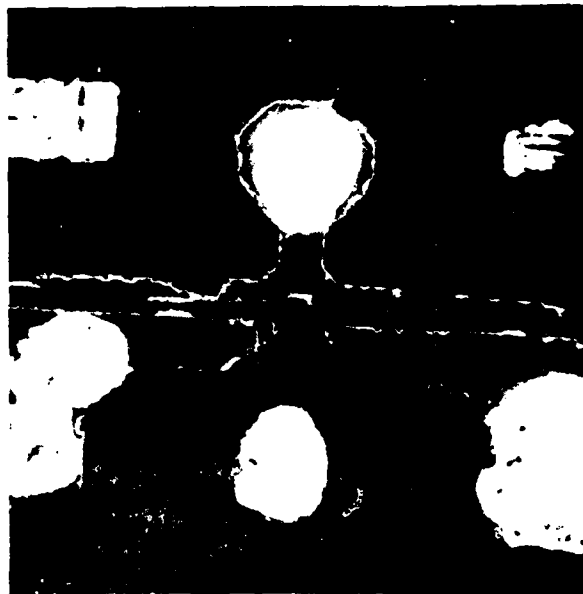
The ohmic contact here appears quite pitted as a consequence of the leaching of the gold from the alloy by the gallium. The pits actually extend into the GaAs surface because the Au-Ge liquid dissolves GaAs during alloying. Figure 3-11(b) shows that the ohmic contact is quite irregular on a microscopic scale. This feature is common to nearly all FETs with a Au-Ge type of alloy contact.

The channel area was carefully examined and was found to be quite clean almost everywhere. One area in the middle of the left gate finger may be partially broken, but we were unable positively to confirm this impression.

To determine if temperature stressing had any observable adverse effect on the ohmic contact metallization, we used the gallium etch method to remove the overlying gold from a Type A-6 FET that had not been subjected to temperature stressing. The appearances of the remaining Ti-W gate metal and of the ohmic contact regions were similar to that of the stressed FET shown in Figures 3-10 and 3-11. Temperature stressing appears to have no significant effect on the contact metallizations of these devices. Additional discussions of gold metallizations are given in Section 5.

In summary, nothing was found in the SEM and EDAX examinations to suggest that metallization failure is the cause of device degradation. If the channel is being compensated by a fast diffusing impurity, it could come from surface or from bulk contamination, or from the gate metal itself. At present, the model of a diffusing impurity which compensates the channel doping seems most plausible.

E2639



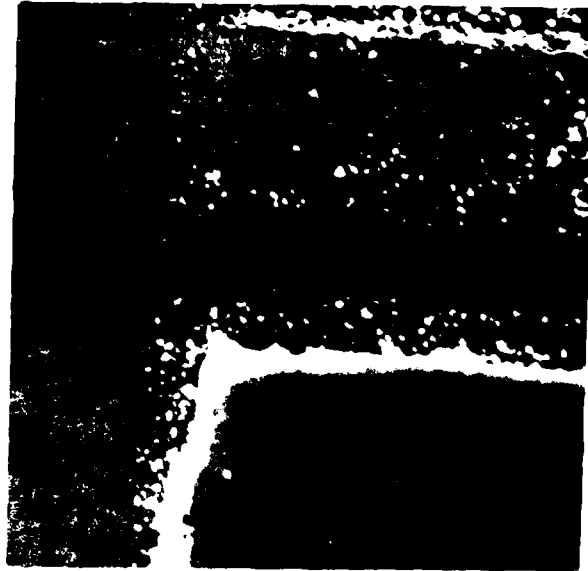
(a)



(b)

Figure 3-10 Type A-6, No. 137, after 533 hours at 260°C, 4 V, 10 mA. Gold removed. (a) Overall view. (b) Detail of gate connector region. The gate metal remaining is Ti-W.

E2640



(a)



(b)

Figure 3-11 Type A-6, No. 137, after 533 hours at 260°C, 4 V, 10 mA. Gold removed. (a) Mesa edge, showing alloyed contact residue. (b) Gate detail. Note etched channel. Gate is 0.8 micrometers long.

3.6 SELECTED HIGH TEMPERATURE STRESS FAILURES

A thorough discussion of device failures in the high temperature stress test is given in the final report for the RADC/Hughes program "Reliability Investigation of Low Noise GaAs FETs."⁽¹⁾ The majority of these failures occurred because some DC electrical parameter, typically the drain current, changed more than the allowable amount. However, a number of other failure modes were also observed. We have selected a representative sampling of the failed devices for discussion in this report. All devices that were subjected to the high temperature stress test were FET chips mounted on a 1 cm by 1 cm carrier.

FETs discussed in this section are the types A-10, D-1, H-1, H-11, and N-3. Devices made by four manufacturers are included, and both gold-based and aluminum gate low noise FETs are represented. The Type H-11 FETs are replacements for the now discontinued Type H-1 FETs. The Type A-10 devices were made by a different manufacturer from the type A-6 devices that were discussed in the previous section. Table 3-3 is a compilation of vendor's data for the grounded source configuration, where standard notations are used for the various parameters. Table 3-4 gives important physical characteristics of these low noise FET chips.

3.6.1 Type A-10 FET

SEM photographs show that the gate region has been etched down in several steps. The gate metal is aluminum, as determined from the EDAX scans. The gate metal edge is ragged, due to the lift-off process. The gate pad is composed of titanium/platinum/gold directly overlaying the aluminum, with a thick gold pad overlaying the titanium/platinum/gold.

EDAX scans of the source metallization show a thick gold bond pad under which is apparently just a titanium/gold layer overlaying what is probably a gold-germanium/nickel alloyed contact. The germanium does not appear on the EDAX scan.

This FET is Device Number 162. It failed as a gate-source short during our periodic room temperature testing sequence, specifically during the automatic network

TABLE 3-3
MANUFACTURER'S SPECIFICATIONS

Type Code	A-10	D-1	H-1	H-11	N-3
<u>TYP. PARAMETERS</u>					
f , GHz	8	8	10	10	8
F_{\min} , dB/ G_a , dB	2.7/9	2.7/8	3.6/6.9	3.2/6.9	2.0/11.5
at I_D , mA/ V_D , V	10/3	20/3.5	12/3.5	12/3.5	10/3
P_O , mW/ G , dB	63/-	-/-	28/-	30/-	7/12
at I_D , mA/ V_D , V	$0.5 I_{DSS}/3$	-/-	30/4	30/4	30/3.0
G_{\max} , dB	11	-	11	11	14
at I_D , mA/ V_D , V	$I_{DSS}/3$	-	60/4	60/4	30/3
I_{DSS} , mA/ V_D , V	80/3	60/3	60/4	60/4	55/3
g_m , mmho	30	35	45	45	25
at I_D , mA/ V_D , V	65/3	60/3	50/4	50/4	30/3
V_P , V	-3	-3	-2	-2	-2.5
at I_D , mA/ V_D , V	100/3	1000/3	100/4	100/4	100/3
θ_j , °C/W	50	70	100	100	170
<u>MAX RATINGS</u>					
V_D , V	5	8	5	11	5
V_G , V	-5	-8	-5	-10	-10
P_{DISS} , mW	500	800	-	-	500
T_{ch} , °C	125	175	125	300	175

NOTE 1: P_O at 1 dB gain compression.

TABLE 3-4
IMPORTANT PHYSICAL CHARACTERISTICS OF LOW NOISE FET CHIPS

Code	Initial Inventory		Gate Metal	Gate Length, μm	Gate Pads	Gate Geometry	Gate Finger Width, μm	Gate Width, μm	Source-Drain Spacing, μm	Source Width, μm	Drain Width, μm	Chip Size, μm
	Chip	Pkg										
A-10	15		Alum.	1.0	1	Two parallel fingers	120	240	4	50	17	305 x 200
D-1	11		Gold	1.0	2	Linear	400	400	5	130	15	500 x 300
H-1	76		Alum.	1.0	1	Linear	400	400	5	85	16	565 x 250
H-11	15		Alum.	1.0	1	Linear	500	500	5	100	20	630 x 310
N-3	61		Alum.	0.5	2	Linear	230	230	2	120	34	360 x 315

analyzer S-parameter measurements. The device had been stressed unbiased at 260°C for 307 hours. As its natural failure time at 260° is unknown, the device failure has to be categorized as a premature "Test/Handling" failure. Severe physiochemical changes in the gate and source metallizations were taking place, however, as will be discussed below.

A SEM photograph of the failed device is shown in Figure 3-12(a). The glass passivation layer is missing near the drain contact. Some roughness is observable on the gate pad, possibly indicating the site of formation of a gold-aluminum inter-metallic compound. However, neither of these situations seems to be directly implicated in the primary failure mechanism of the FET, and they will not be considered further. The problem of FETs that have the gold-aluminum intermetallic compound is discussed in Sections 3.6.3 and 5.3.

The primary failure site is located by the arrow near the left source bond wire in Figure 3-12(a). The failure is attributable to the growth of metal nodules between the gate and source metallizations, as shown in Figure 3-12(b). Note the closeness of the gate metallization and the source electrode. The raggedness of the edges of the gate metallization is apparent in this photograph. It is possible that a combination of electrode proximity and locally severe rough gate metal edges precipitated failure at this particular site.

The discolorations shown in Figure 3-12(b) in the surfaces of the gate and source metallizations were investigated using the EDAX capability of the SEM. The EDAX feature allows a scan to be performed for only one element. Presence of the designated element results in a white dot in the SEM photograph. Thus, a map is obtained showing where the selected element is found.

Figure 3-13(a) shows an aluminum mapping at approximately the same location and magnification of Figure 3-12(b). Note that the large nodule in Figure 3-12(b) has a high percentage of aluminum. The aluminum has largely disappeared from the gate stripe near the top of the photograph and apparently has migrated to form the nodule. These devices were stressed unbiased at 260°C for 307 hours.

E2941



(a)



(b)

Figure 3-12 SEM photographs of the failed Type A-10, No. 162 FET. (a) 300X; (b) 12,000X.

E2942



(a)



(b)

Figure 3-13 Type A-10, No. 162 FET. SEM/EDAX mappings at 12,000X of the failure site shown in Figure 3-12(b).
(a) Aluminum; (b) Gold.

A gold mapping of the same region is shown in Figure 3-13(b). The darker area on the source contact in Figures 3-12(b) and 3-13(b) thus corresponds to an area of reduced gold content. The gold atoms have migrated to the aluminum gate stripe, forming a nodule and intermetallic compounds.

Suggestions for increasing the reliability of the Type A-10 FETs include improvement of the lift-off process for forming the gate metal, more careful placement of the gate electrode to avoid too close proximity with the source and drain electrodes, and better design of the refractory metallization layer to inhibit gold migration.

3.6.2 Type D-1 FET

This is a gold gate FET, our Device Number 100. It was stressed biased at 240°C and failed in the oven by a gate-drain short at 1095 hours. The failure was observed as an inability to control the drain current with gate bias. Figure 3-14(a) shows a SEM photograph of the failed FET with the failure site identified by an arrow. A close-up view of the gate-drain short is shown in Figure 3-14(b).

A SEM photograph of a portion of the gate stripe is shown in Figure 3-15(a). A darker, discolored area is shown that is typical of other discolored areas on the gate stripe. A SEM/EDAX gold mapping of this area is shown in Figure 3-15(b). The light regions show the presence of gold. It can be seen that the discolored area is a region having less gold.

Considerable mottling of the gate pads is apparent in Figure 3-14(a). Similar mottling of a medium power FET made by the same manufacturer has also been observed. Those findings are discussed in Section 4.3.2 and seem to apply also to the Type D-1 FET. Compare also Figure 3-20(b). A better gold-based gate metallization would improve the reliability of the Type D-1 FET.

3.6.3 Type H-1 FET

The Type H-1 FET has an aluminum gate metallization. The gate is etched down into the channel and, as indicated by the SEM photos prior to removal of the glass, was apparently formed by lift-off. The gate is nearly in the center of the channel with a

E2943



(a)

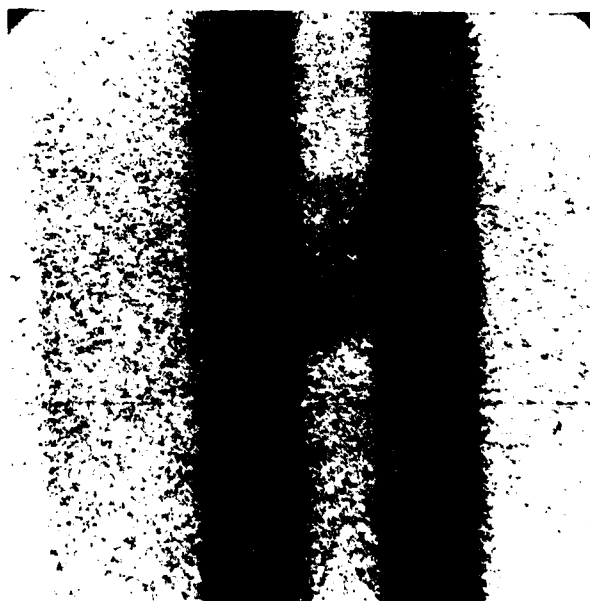


(b)

Figure 3-14 SEM photographs of the failed Type D-1, No. 100 FET. (a) 198X; (b) 900X.



(a)



(b)

Figure 3-15 Type D-1, No. 100 FET. (a) SEM photograph of a portion of the gate stripe showing discoloration (9000X); (b) EDAX gold mapping of the same area.

very slight offset toward the source side. The gate pad is composed of a gold metallization over aluminum, and the EDAX scan does not show any other metals. However, we know that the gold is separated from the aluminum by a refractory layer. One unusual aspect is that the scan of the ohmic contact shows the presence of chromium as well as nickel. The device has a fairly sharp mesa step, but it is less than the thickness of the gate metallization. The gate stripe does not have an enlarged area at the ends and is also not constricted where it passes over the mesa edge. This uniformity at the mesa edge is probably a result of the use of a relatively shallow mesa etch.

The FET discussed here, our Device Number 44, was stressed biased at an oven temperature of 220°C. The device failed after 263 hours by exceeding the allowed percentage change in drain current. However, the FET was kept on test beyond 263 hours to accentuate the failure mode. The pictures shown were taken after 1590 hours at 220°C.

Figure 3-16 shows an overall photograph of the failed FET and a close-up view of the gate pad to gate transition region. For ease in observing the device we removed the gate bond wire and bent the other wires down. The bond wires were not participants in the failure mechanism. The failure is due to the formation of the gold-aluminum intermetallic compound commonly called "purple plague".

Figure 3-17(a) shows a view of the gold gate pad and aluminum transition. The intermetallic compound formation is extensive. Figure 3-17(b) is an EDAX mapping for aluminum. In the transition region, voids in the aluminum metallization are clearly evident. In the pad region, incursions of aluminum atoms into the gold pad region can be seen around the periphery of the pad and near the bond wire site.

The corresponding gold mapping is shown in Figure 3-17(c). Note a region near the gate bond wire site where neither aluminum nor gold is present. We did not pursue this observation further, however. Also observable near the lower left hand corner of Figure 3-17(c) is a void in the edge of the gold ohmic contact layer of the drain near the gate stripe.

E2945



(a)



(b)

Figure 3-16 (a) SEM photograph of failed Type H-1, No. 44 FET at 102X; (b) Close-up view of the gate pad to gate transition region, showing pitted aluminum and gold-aluminum intermetallic compound. 1500X.

E2946



Figure 3-17(a) Type H-1, No. 44 FET. Gold gate pad and aluminum transition at 250X.

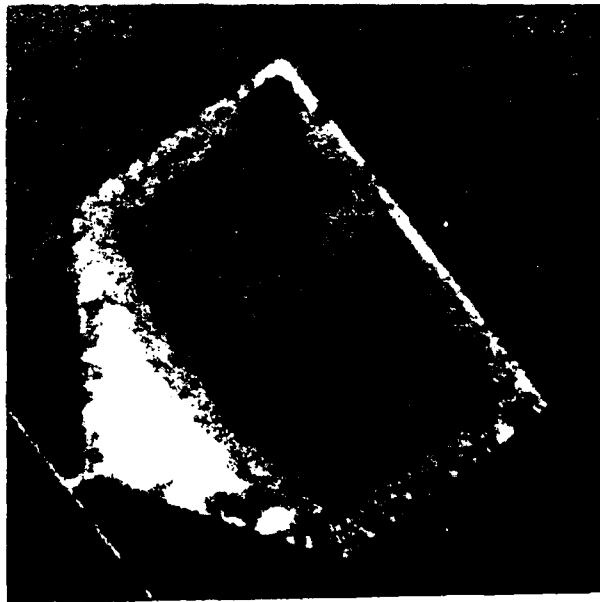


Figure 3-17(b) Aluminum mapping of the failed Type H-1, No. 44 FET.

E2947



Figure 3-17(c) Gold mapping of the failed Type H-1,
No. 44 FET.

As stated earlier, this FET was kept on test well beyond the time of the degradation failure that occurred at 263 hours. Eventually the device failed catastrophically at 1590 hours by a gate short at the site indicated by the arrow in Figure 3-16(a). Note that the overlay glass is missing in this area over the gate and source and appears only over the drain metallization.

A close-up view of the gate failure site is shown in Figure 3-18(a). Figure 3-18(b) shows a gold mapping of the same area. Clearly, gold has disappeared from the source and drain metallizations and appears in the gate region at the site of the short. An aluminum mapping of the same area indicates that the aluminum gate stripe metallization is interrupted in the vicinity of the short.

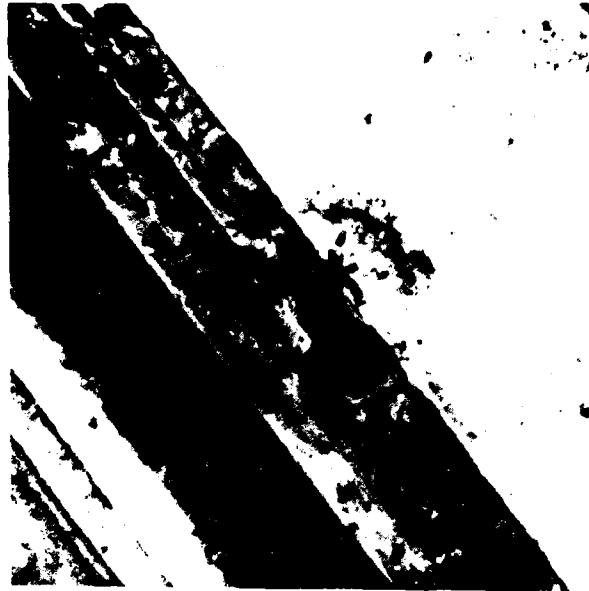
Metal migration was found to be a widespread problem in the Type H-1 FETs, especially with the gate pads. Consequently, a special failure mechanism study was inaugurated to examine the degradation of the gold-aluminum gate pads. Intermetallic compound formation due to damaging the refractory interlayer in bonding was the focus of the study. Results are given in Section 5.3.

Another reliability problem with the Type H-1 FETs was encountered in die bonding. The dice were found to be brittle and broke up readily when our operators were in process of mounting the FET chips. We contacted the supplier regarding the reliability of the Type H-1 devices. We were informed that the Type H-1 FETs were being discontinued. The manufacturer then sent us samples of the improved device, the Type H-11 FET. We were able to accommodate limited testing of the Type H-11 devices. We discuss their results next.

3.6.4 Type H-11 FET

The Type H-11 device is similar in appearance to the Type H-1 FET. Improvements were made in the processing of the FET. Our Device Number 183 was selected for discussion in this section. The FET was stressed biased for 48 hours at 260°C. An overall photograph of the failed FET is shown in Figure 3-19(a). Again, for ease in observation we removed the gate bond wire and bent the other wires down. These wires were not implicated in device failure.

E2948



(a)



(b)

Figure 3-18 Type H-1, No. 44 FET. (a) 2000X view of the gate short failure site in Figure 3-16(a); (b) Gold mapping, showing gold migration from the source and drain metallizations to the gate region.

Failure of the device was indicated in the oven by loss of ability of the gate to control the drain current. The site of gate failure is shown by the arrow in Figure 3-19(a). A close-up view of the failure site is shown in Figure 3-19(b). The glass remained intact. The failure appears to be due to gold migration from the source and drain metallizations.

No gold-aluminum intermetallic compound formation was observed. The aluminum/gold pad metallizations showed no obvious degradation. However, widespread degradation was observed in the gold metallization around the periphery of the source and drain ohmic contacts. Voids and nodules formed, as shown in Figure 3-20. Dark spots observed on D-type FETs are discussed in Sections 3.6.2 and 5.3.

Our recommendation for improving the reliability of the Type H-11 FET is obvious: Continue to improve the metallization processes.

3.6.5 Type N-3 FET

The gate of this device is aluminum, and it is connected to a gold pad by a titanium/platinum overlay metallization. The gold does not overlay the aluminum. Scans of the ohmic contact show only platinum without any traces of the gold or germanium. This finding is probably an artifact of the EDAX measurement, as it is known that the gold-germanium alloyed contact is used for this process. On one sample we removed the gate, and we were able to observe that there was no etching of the GaAs prior to the deposition of the gate. This construction is in accord with the use of the self-aligned process. However, a photograph of the gate electrode on the sample taken prior to removal of the glass showed clearly that the gate was not in contact with the GaAs where it crossed the mesa step and was considerably narrowed there. The gate also showed evidence of some etching prior to deposition of the titanium/platinum overlay connector.

We discuss here our Device Number 8, which was stressed biased at 200°C. The symptom of impending failure was a substantial increase in gate current. The device actually failed with a gate short during DC testing after 881 hours. We consider in this case, however, that the real failure mechanism was the conditions that led to the increase in gate current.

E2949

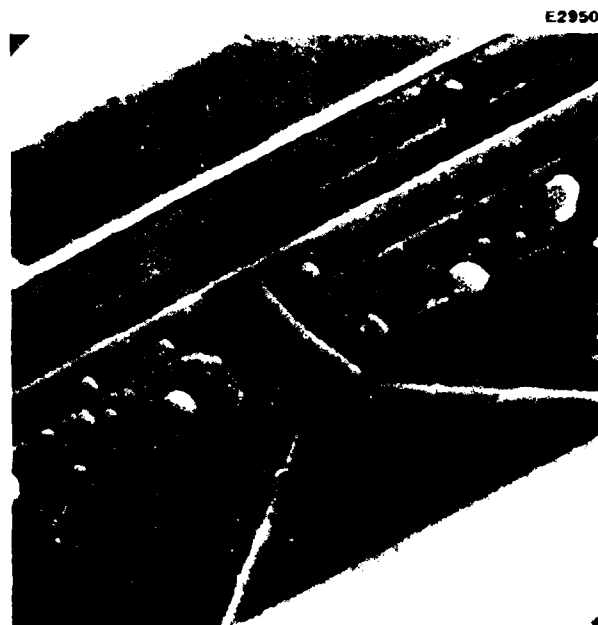


(a)

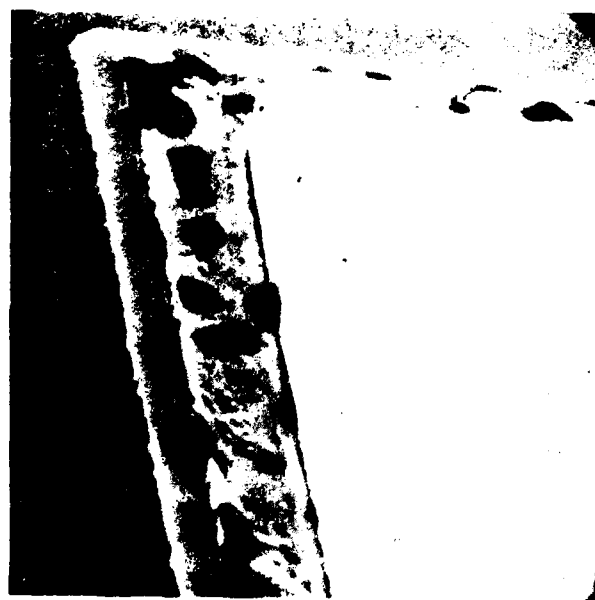


(b)

Figure 3-19 (a) SEM photograph of the failed Type H-11, No. 183 FET at 150X; (b) 6000X view of the gate failure site.



(a)



(b)

Figure 3-20 Type H-11, No. 183 FET. (a) SEM photograph at 2500X of the gate pad to gate stripe transition showing metallization voids and nodules; (b) 6000X photograph of the upper left corner of the drain contact pad in Figure 3-19(a).

Figure 3-21(a) shows an overall SEM photograph of the failed FET. The bonding wire to the right gate pad has been moved aside to give an unobstructed view of the region. Close examination of the gate disclosed the presence of nodules on the gate stripe in several places. An enlarged view of one of the nodule regions on the gate stripe is shown in Figure 3-21(b). EDAX scans of the nodules show them to be composed of aluminum and gold with some gallium present.

As is the case for a number of other FET types, improved metallization techniques are a key to better reliability of the Type N-3 FET.

A discussion of results of the 120°C stress test of a packaged Type N-3 FET is given in Section 3.7.

3.7 MEDIUM TEMPERATURE STRESS TEST FAILURES

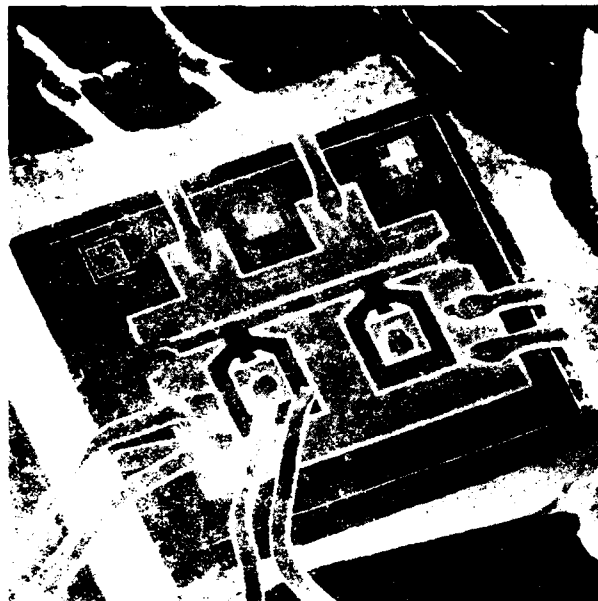
A discussion of the medium temperature constant stress tests, which was done on packaged devices, is given in the final report for the RADC/Hughes program "Reliability Investigation of Low Noise GaAs FETs".⁽¹⁾ As explained in that report, we have anticipated a possible low failure rate under test. Of 53 FETs started, only six have failed so far in test. This stress test is being continued.

The test consists of stressing eight device types representing five manufacturers at two temperatures, 85°C and 120°C. No one device type at a given temperature had more than one failed FET represented among the six failed units. Five of the failures were categorized as a gate short. Four of these five were biased.

We have selected for presentation in this section one of the gate short failures of biased devices. Our packaged Device Number 38 is a Type N-32 FET, which is a packaged Type N-3 FET. It was stressed biased at 120°C and failed after 96 hours in the oven. The symptom of failure was a gate-to-source short circuit.

The package was delidded, and a color photograph was made of the FET. We found extensive deterioration of the source, gate, and drain metallizations due to the formation of the gold-aluminum intermetallic compound, or "purple plague". The

E2981



(a)



(b)

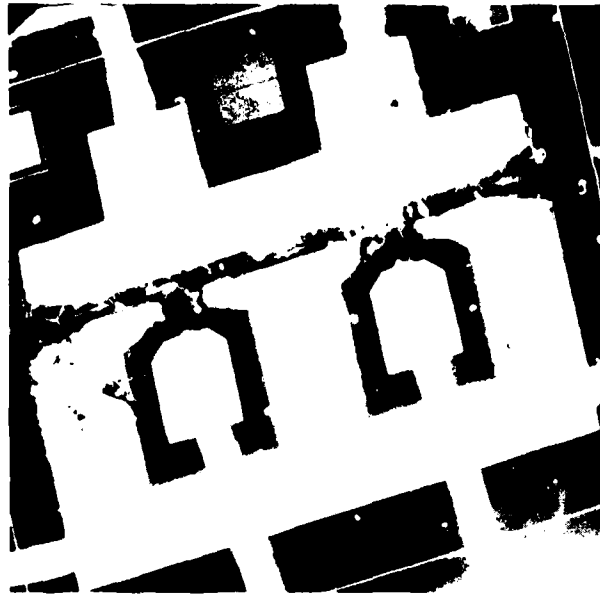
Figure 3-21 (a) SEM photograph of failed Type N-3, No. 8 FET at 160X; (b) Nodules on the gate stripe. 12,000X.

intermetallic compound also extended a considerable distance along the drain bond wires.

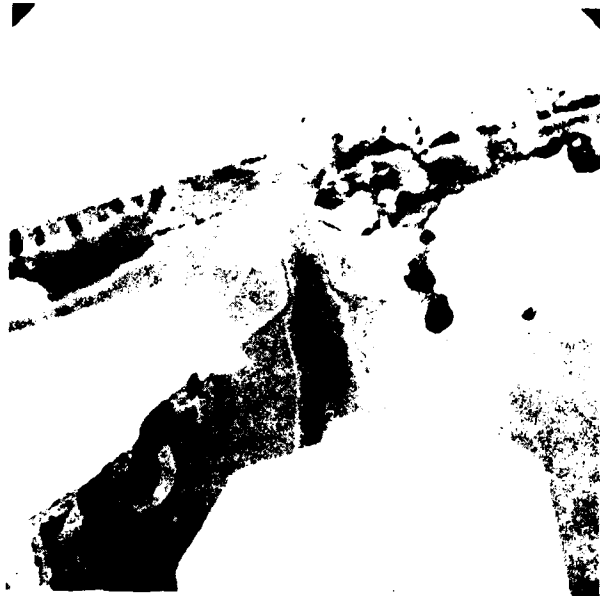
An overall SEM photograph of the failed FET is shown in Figure 3-22(a). Figure 3-22(b) shows a close-up photograph of the left gate pad transition. The photographs show the gold-aluminum intermetallic compound formation on the three electrodes and drain bond wires.

A discussion of results of the 200°C stress test of the Type N-3 chip is given in Section 3.6.5. To increase the reliability of the Type N-32 packaged FET, not only must due consideration be given to improving the metallization of the device, but also the atmosphere inside the package needs to be examined.

E2952



(a)



(b)

Figure 3-22 (a) SEM photograph of failed packaged Type N-32, No. 38 FET at 390X; (b) Close-up view of the left gate pad transition showing the gold-aluminum intermetallic compound formation involving source, gate, and drain metallizations. 1200X.

4.0 FAILURE ANALYSIS OF MEDIUM POWER DEVICES

4.1 RADC/TI MEDIUM POWER GaAs FET RELIABILITY PROGRAM

RADC has funded a program at Texas Instruments (TI) to study the reliability of medium power FETs.⁽²⁾ Failed devices were delivered to RADC for further analysis and characterization. Many of these devices were then delivered to Hughes for evaluation on the present program. In this section we present the information that we have received concerning the devices. For more thorough coverage of the device tests and observations of failures, the interested reader is referred to the relevant RADC/TI reports.

4.2 MAXIMUM ELECTRICAL LIMITS

Table 4-1 gives a listing of maximum-stress tested devices received from RADC, the tests to which they were subjected by TI, and the evaluation tests performed on them by Hughes. These tests were all carried out to determine maximum electrical limits, and all the failures were catastrophic.

In Section 4.2.1 we give a rather narrative report and tables on the Type T-500/8 FETs. These devices are built with Al gate electrodes, as are the Type N-250/11-P devices. The Type D and Type M devices used a Au-based gate metallization. We concentrated on the Type T and Type D FETs because they represented the Al and Au gates and because there was not evidence to suggest substantial differences in the information among all four device types. Also, in the Type M FETs the gate electrode is essentially obscured by the source and drain edges. Thus, it is nearly impossible to inspect the gate either by optical or SEM methods. We did remove the gold from one of the Type M devices to get a better look at the device geometry.

We now present a detailed discussion of the failures observed on the Type T-500/8 devices. These were the first to be analyzed, but they were later found to be quite typical of the other devices. Then, we discuss the results in terms of the categories of tests performed by TI.

TABLE 4-1
RADF-FURNISHED POWER FETS EVALUATED

DEVICE TYPE, NO.	TI TEST ¹	HUGHES EVAL. ²	DEVICE TYPE, NO.	TI TEST ¹	HUGHES EVAL. ²
<u>T-500/8</u>			<u>D-250/6</u>		
1	A	S,E,O	4	A	S
2	A	S,E,O	11	B	S
3	D	S	12	B	S
4	D	S	13	C	S
5	E	S	14	C	S
6	E	S,E,O	18	E	S
8	B	S,E,O	21	E	S
9	B	S	22	D	---
10	B	S	23	D	S
11	C	S			
12	C	S			
<u>N-250/11-P</u>			<u>M-400/6</u>		
1	A	S	2	A	---
33	A	---	3	B	S,O
23	B	S	6	B	---
5	B	S	7	C	---
4	C	---	8	C	S,O
30	C	---	9	E	---
9	E	S	10	E	S,O
28	E	---	11	D	S,O
27	D	---	12	D	---
25	D	S			

- Notes: 1. A: Maximum Drain Voltage ($V_G = 0$)
B: Maximum Reverse Gate Voltage
C: Maximum Gate Forward Current
D: Maximum Drain Voltage Under Operating Conditions
E: Maximum CW RF Input Power
2. S: SEM Topograph
E: EDAX Scan, selected areas
O: Optical Microscopy

4.2.1 Example: Type T-500/8 FET vs Tests

The following is a narrative description of the failure modes observed in the T-500/8 power FETs that failed during electrical stress tests. Eleven failed T-500/8 FET devices were received for failure analysis. Seven of the packages had been opened and showed evidence of SEM evaluation. The overlay SiO_2 layer had been removed on four of the seven opened units, presumably for a more extensive SEM/EDAX procedure. The four unopened devices were exposed for evaluation by mechanically removing the package lid. Scanning electron microscope photographs were taken at appropriate magnifications and were complemented with EDAX analyses where desirable.

Table 4-2 gives a summary of the device failure modes and test conditions while Table 4-3 gives more detailed comments on the failure sites and EDAX results.

Figure 4-1 shows a Type T-500/8 device that failed in the maximum drain voltage test, Test A. This figure should be compared with Figure 4-2, which shows another device of the same kind. In each photograph the failure site is apparent. In Figure 4-1 the device has been etched, probably in a plasma stripper, so that the passivation is removed. In Figure 4-2 note the debris on the surface. Also, note the balls of material at the failure sites. These globules apparently have been removed by the etching process for the FET of Figure 4-1, along with the clear scratch protection layer. This layer is seen in the drain and gate areas of Figure 4-2.

Unfortunately, we can conclude little as to the mode or reason for failure of these devices, other than in simple terms. The failure is probably due to overvoltage between the gate and drain, but the resulting destruction of the device leaves little to observe. Obviously, destruction of the ohmic contact and gate electrodes is involved. Some GaAs also melted and dissolved into the failure region.

In Figure 4-1 only the gate and drain are involved, and this fact is our evidence for supposing that the failure is usually between gate and drain. On other failure sites, however, all the electrodes are involved. Also, note that the germanium-rich hillocks in the Au-Ge contact are removed by the (presumed) plasma etching process (compare Figure 4-1 and 4-2).

TABLE 4-2
SUMMARY OF DEVICE FAILURE MODES, T-500/8

Device No.	Test Conditions	Failure Mode
1	Maximum V_{DS} , $V_G = 0$	Alloyed crater from gate pad to drain.
2	Same	Alloyed crater from gate pad to source.
3	Maximum V_{DS} Under Operating Conditions	Alloyed crater from gate pad to source.
4	Same	Alloyed crater from gate pad to drain.
5	Maximum CW RF Input	Obscure gate failure under a source wire bond cross over. Alloyed crater.
6	Same	Alloyed crater from gate pad to source.
8	Maximum - V_G	Alloyed crater between source and drain with a spherical ball of resolidified material.
9	Same	Alloyed crater between gate pad, source, and drain.
10	Same	Alloyed crater between gate pad, source, and drain.
11	Maximum $+I_G$	Alloyed crater between source and drain.
12	Same	Alloyed crater between gate and source.

TABLE 4-3
FAILURE MODE DETAIL, T-500/8

Device No.	Failure Mode
1	Shows crater at gate feed from gate pad to drain metallization. Crater has obviously lost material by ejection which is not to be found due to subsequent (assumed) sputter process removal of SiO ₂ overlay by Ti. EDAX of resolidified crater showed GaAs, Au and trace Ni, trace Ti.
2	Shows crater at gate feed to source metallization. Crater ejecta are present, as no attempt was made to remove SiO ₂ overlay. Preferred site is mesa edge at gate pad, but one site is in mid-finger. EDAX of gate ejecta sphere showed Au as major constituent, Ni, Ti, Cr as trace.
3	Same as (2) - No EDAX performed.
4	Same as (1) - No EDAX performed.
5	A subtle, almost obscured gate failure under a source wire bond crossover. Failure was cratered and ejecta were missing due to SiO ₂ overlay removal. Damage occurred largely in one place, with several other shorts between gate and drain on same finger. No EDAX performed.
6	A large area alloyed crater that involves the entire end of gate pad and spreads to the source metallization. EDAX of resolidified crater showed GaAs, Au, trace Si, trace Ti, trace Ni. This failure is the largest in extent of any observed and terminates at gate bond wire.
8	Alloyed crater between source-drain that involves the gate. A gate ejecta sphere EDAX showed GaAs, Au, trace Ni, trace Ti, no Cr was found. This was the only case analyzed in which the passivation was removed (by Hughes) and the ejecta sphere remained.
9	Alloyed crater at gate feed to source and drain metallizations. No EDAX performed.
10	Same as (9), except this is the only case where the drain finger was destroyed.
11	A large area alloyed crater that involves the gate pad and the source metallization. No EDAX performed.
12	Alloyed crater from gate to source metallization. No EDAX.

E2524

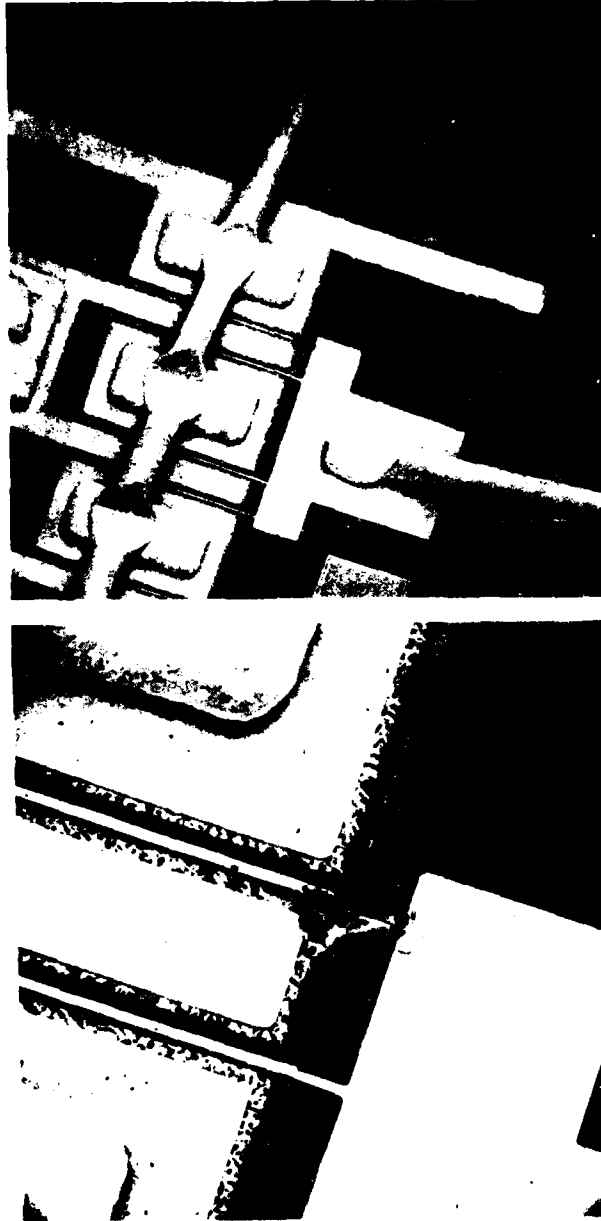


Figure 4-1 Type T-500/8, #1, after
maximum V_{DS} , $V_G = 0$;
electrical stress test.
SEM at 200X, 1000X.

E2525



Figure 4-2 Type T-500/8, #2, after
maximum V_{DS} , $V_G = 0$;
electrical stress test.
SEM at 200X, 400X.

In general, the failure analyses of these devices led to little in the way of information that would suggest improved methods of device fabrication, screening techniques, or specific reasons for failure. The failure mode was obviously catastrophic in every case, and the resulting energy dissipation caused so much damage that very little of the assumed incipient damage site remains.

Inspection of the undamaged portions of the devices reveals small defects in the channels which could be sites for failure. However, without additional testing it is impossible to make any more exact determination.

4.2.2 Comparison of Failures vs. Test Method

In the following paragraphs we summarize our observations, categorizing them by the stress test, then by device.

Maximum Drain Voltage (Test A)

We assume that this test is made under DC conditions, with $V_G = 0$, as noted. The Type N-250/11-P (the P refers to packaged) FET failed by fusing the drain wire open. There was no overt damage to the device. We have not probed the cell to see if it is still good. We noted with interest that these Type N FET packages all contained a chip with two cells, only one of which was connected. We have not checked to see if the unbonded cell is good.

The Type T FET failures were catastrophic, involving fused gate fingers near the gate pad and within the unit cell. These failures were shown in Figures 4-1 and 4-2.

In the Type D device there was no overt failure site, Figure 4-3. Further tests would be needed to completely characterize the failure. The black spots appearing in the gallium arsenide and in the metallization should be noted. See Section 4.3.2 for a discussion of black spots in the metallization. The discolorations in the gallium arsenide were not investigated directly.

AD-A104 440

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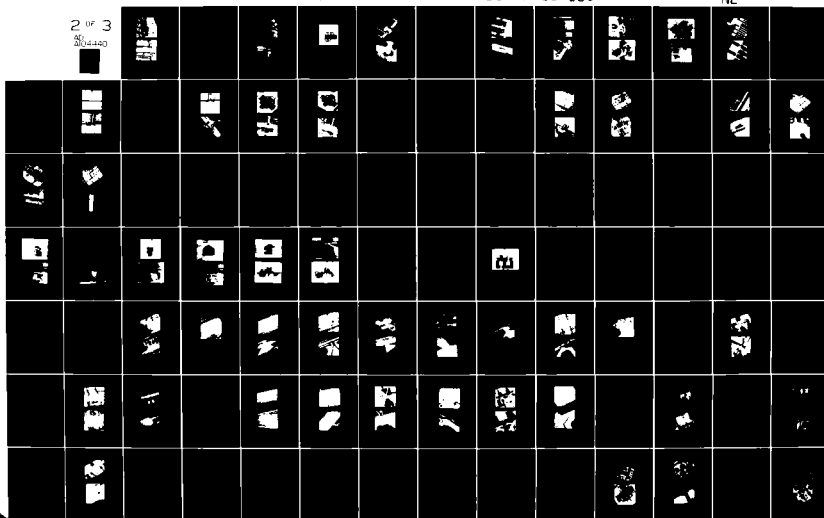
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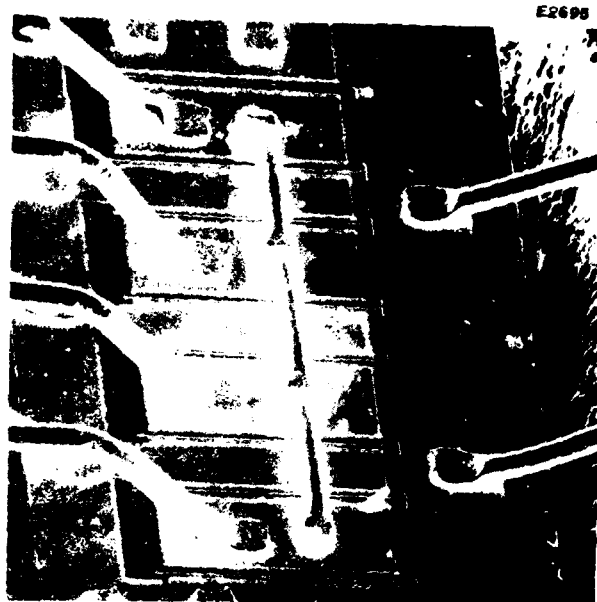
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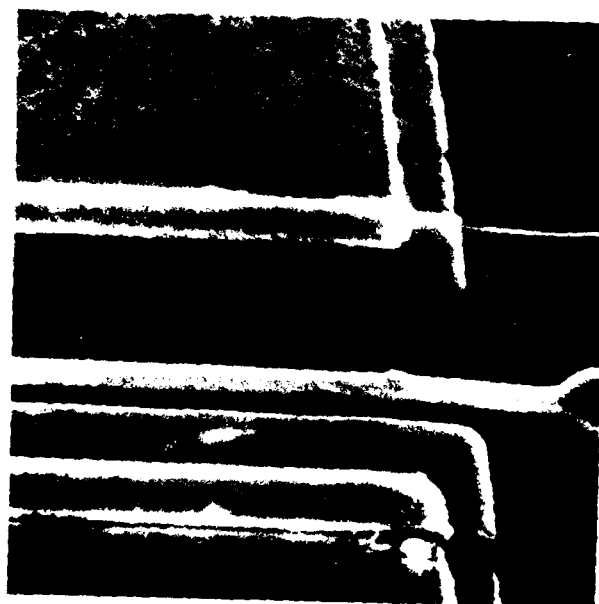
2 of 3

204440





(a)



(b)

Figure 4-3 Type D-250/6, FET from Test A. (a) 200X, note cracked die. (b) 4000X, note black spots.

Maximum Reverse Gate Voltage (Test B)

All failures for this test were catastrophic. We assume that the test was done under DC conditions. Except for the Type T FET, the failures involved the gate pad-to-finger junction, as well as the source and drain in most cases. In the Type T FET the primary failure appeared to be mid-channel, with the drain finger fused in one case. The Type D FET also had one of the two parallel gate wires burned in two, Figure 4-4. In this case we were able to remove the glass with minimal etching, if any, of the other metallization using the fumes of concentrated HF.

Burn-out of the gate wire indicates that the current probably was not limited to a low enough value in these tests. To do so would require resistive limiting close enough to the chip that parallel capacitive energy storage would be minimized. One could also use GaAs FETs as limiters.

Finally, Figure 4-5 shows a Type M FET that has been removed from its carrier for evaluation. In this case the Au pads remained on the carrier. The failed area is the darkened gate electrode.

Maximum Gate Forward Current (C)

Here again, all the failures were catastrophic, involving source, gate and drain. In every case, the gate pad or gate pad-to-gate-finger junction was involved. The metals of all three were usually fused together at that point.

Figure 4-6 shows examples of the catastrophic damage involved for Types D and T FETs. In these two cases the gate and source are primarily involved.

Maximum Drain Voltage Under Operating Conditions (D)

There was more variability in the failures on this and on the following tests than on the preceding two tests. We assumed that the tests were carried out with the FET operating under RF drive, in both cases D and E. In many cases the failure site exhibited the kind of appearance one associates with an arc weld. We called it a "flashover" type of failure, in contrast with the A, B, and C tests. In those cases we observed metal balls and eruptions as residue of the failure.

E2696



(a)



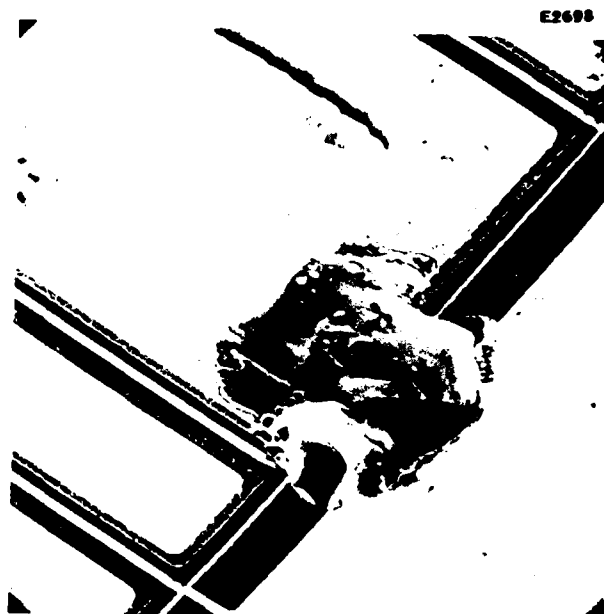
(b)

Figure 4-4 Type D-250/6 FET, from Test B.
(a) 200X, showing burned gate wire. (b) Gate burnout. HF was used to remove the glass without removing all of the debris.

E2697



Figure 4-5 Type M-400/6, #3,
from Test B.



(a)



(b)

Figure 4-6 (a) Type T-500/8, #11, at 1000X. (b) Type D-250/6, #14, at 2000X.

In the Type D FETs, Figure 4-7, the failures were in mid-channel and caused the gate electrode to be lifted away, nearly intact, from the GaAs. Damage to the GaAs was not extensive, with clear evidence of the etched gate trough still visible. The Type N failure, Figure 4-8, had an appearance similar to those of Tests A, B, and C, but with more of the "flashover" appearance. Shown also is a Type T FET. The failure site was from the gate pad/gate finger junction to the drain.

The Type M FET failure, Figure 4-9, was of the "flashover" type at the gate pad. Though we could not see the site well, there was some evidence that the gate finger had erupted, also. This device also exhibited the "flashover" effect from the gate pad to the source and drain.

Maximum CW RF Input Power (E)

In the cases of the Type M, D and T FETs, Figure 4-10, the predominant failures were all of the "flashover" type, with smaller failures elsewhere. Primary site was at the gate pad/gate finger junction, again. In the Type N FET, Figure 4-11, the failure caused two source fingers to be melted, with those fingers not apparently shorted to the gate or drain.

4.2.3 Summary Comments

Several comments on the data are in order. The failures were nearly all catastrophic and resulted in the three device electrodes being shorted together. The two exceptions were the Type N devices, which opened a drain wire on test A and opened individual fingers in test E. This may mean that the device metal is not thick enough (not enough bond wires, also) to transfer the electrical stress to the semiconductor. The other devices appear to fail when the intrinsic device, either in the bulk or on the surface, fails. Of course, there is no way to discover from these tests what the role of process defects may be.

We suggest that such tests should be carried out with more care, if feasible, to limit the energy input following failure initiation. The practicality of this desire may be argued, but we feel that the problems are not insurmountable for DC tests. With RF tests, limiting RF power levels is difficult, given the probable very short time constants of the faults.

E2699



(a)



(b)

Figure 4-7 Type D-250/6, #22, from Test D. (a) 400X, showing location of burn-out in mid-finger. (b) 4000X, showing lifted gate and replica in passivating glass.

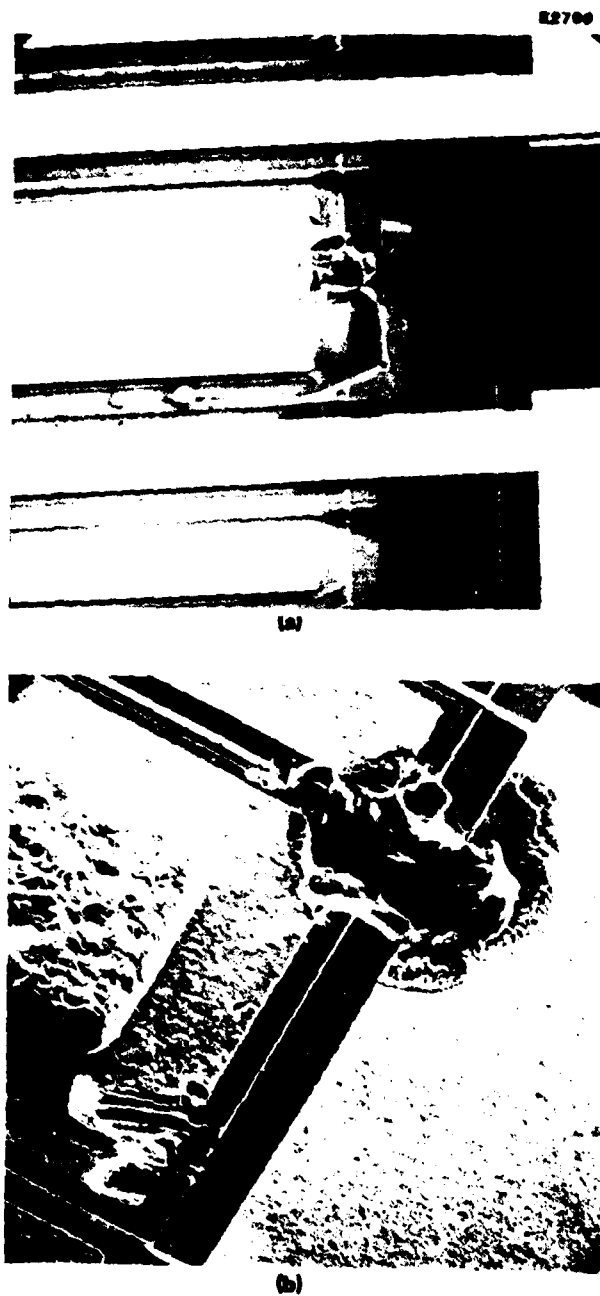


Figure 4-8 (a) Type N-250/11-P, #25, Test D, 200X. (b) Type T-500/8, #4, Test D, 1000X.

E2701



(a)

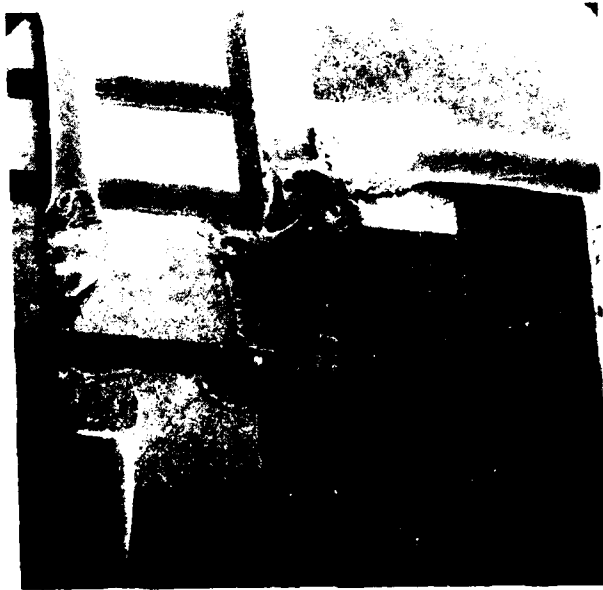


(b)

Figure 4-9 Type M-400/6, #11, Test D. (a) Optical photograph (color original) at 500X. At the top of the photograph note one source pad which remained on-chip after prying of the chip from the heat sink. (b) SEM photograph.

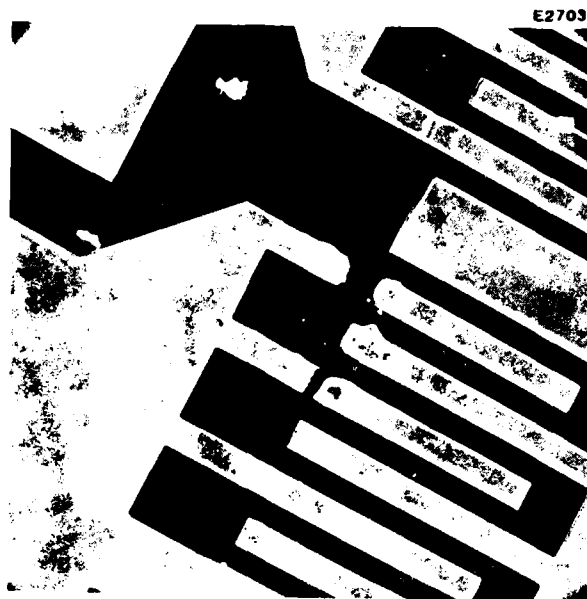


(a)



(b)

Figure 4-10 (a) Type M-400/6, #10, Test E, 1000X. (b) Type D-250/6, #21, Test E, 400X.



(a)



(b)

Figure 4-11 Type N-250/11-P, #9, Test E.
(a) 400X. (b) 1000X. Note
melted source fingers, with
some melting of the drain
finger.

4.3 TEMPERATURE STRESS TEST

At TI a number of medium power FETs were held under bias at elevated temperatures for periods of time ranging to over 1500 hours. Failed devices were sent to RADC, and RADC delivered six Type M-400/6 devices and seven Type D-250/6 devices to Hughes for failure analysis.

Delivery of the devices was accompanied with a brief statement concerning the failure conditions and observations. Information on the Type M-400/6 FETs is given in Table 4-4, and information on the Type D-250/6 FETs is given in Section 4.3.2.

4.3.1 Type M-400/6 FETs

Type M-400/6 devices are medium power FETs with eight gate fingers, four drain fingers, and five source pads. The FET is flip-chip mounted to a heatsink and sealed in the package.

All the Type M devices were packaged, and we opened them for analysis as required. The type M chip is flip-chip bonded to its heat sink. In every case we found it simple to remove the chip by prying it up along one long edge. The gold plated source pads, which are thermocompression bonded to the copper heat sink, usually separated from the chip. In some cases one or two pads stayed on the FET chip. In no case was the GaAs torn out of the chip by the source pads. The metallization apparently separated along one of the layers, but not gold, judging from the color. In cases where the pad stayed on the chip, it appeared that the pad surface had not been much disturbed by the bonding. This observation suggests that the device heat distribution could be seriously upset by poorly bonded pads. We suggest that, in critical applications, the temperature uniformity of the operating chip backside be monitored as a screen against poorly bonded source pads.

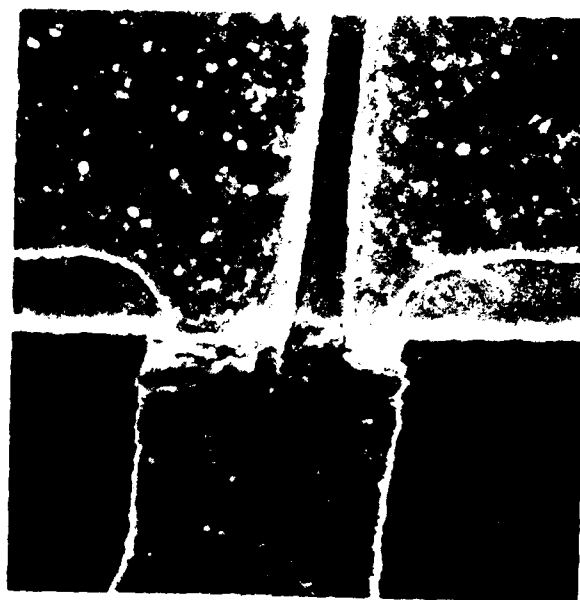
SEM photographs of the 12J device are shown in Figure 4-12. Two gate fingers with intervening drain electrode, along with a source electrode with torn metallization, can be observed in Figure 4-12(a). A close view of the gate finger is shown in Figure 4-12 (b), where voids and raggedness are apparent in the gate metallization.

TABLE 4-4
CHARACTERISTICS OF FAILED TYPE M-400/6 DEVICES
RECEIVED FROM RADC

Device Number	Drain Voltage (V)	Drain Current (mA)	Heatsink Temperature (°C)	Observation
9J	8	150	200	P _{out} drops slowly; 1 dB down after 301 hours.
10J	8	150	200	P _{out} dropped to near zero in several discrete steps starting at 30 hours. Each step (each power level) lasted for 1-5 hours. I-V characteristic did not change by a large amount.
12J	8	150	200	Similar to 10J - started after 54 hours.
13J	8	145	185	P _{out} degraded 1 dB after 140 hours--I _{DSS} decreased from 365 to 320 mA. I _G unchanged.
14J	8	145	185	P _{out} degraded 1 dB after 200 hours--I _{DSS} decreased from 360 to 270 mA. Max g _m decreased from 105 to 80 mmho. I _G unchanged.
15J	8	145	185	P _{out} degraded 1 dB after 133 hours--I _{DSS} decreased from 380 to 360 mA. I _G unchanged.



(a)



(b)

Figure 4-12 SEM photographs of the Type M-400/6 12J device. (a) 1500X; (b) 6000X.

Devices 9J and 10J exhibit gate metallization problems similar to those of device 12J. Figure 4-13(a) shows a gate pad and finger with metallization voids, device 9J. Figure 4-13(b) depicts another gate pad and finger transition on the same device, showing metallization voids and a tenuous transition across the gallium arsenide step from gate pad to the recessed gate finger. SEM photographs of the 10J device are not included in this report, as they show similar features to those depicted in Figures 4-12 and 4-13.

The reported failure modes of devices 13J, 14J, and 15J are similar to those of the 9J, 10J and 12J devices, although, as expected, devices stressed at the lower temperature tended to last longer. Of these, only the 14J was additionally selected for close examination. SEM examination again showed voids in the gold of the gate pad transition and adjacent gate stripe.

SEM photographs of the 14J device are shown in Figure 4-14. Figure 4-14(a) shows the overall view of the chip after it had been demounted from its heatsink. The gate electrode is on the left, and the drain pad is on the right. The five source pads for flip-chip mounting are also clearly visible. Dust particles as a result of handling are visible and should be ignored. The arrow points to the spot where the close-up view of the gate pad to gate stripe transition was taken that is shown in Figure 4-14(b).

Figures 4-12, 4-13, and 4-14 all show problems with the gate metallization on the stressed FETs in the vicinity of the mesa step. To help determine whether the voids occurred as a result of the manufacturing process or from temperature stressing, we examined a new Type M-400/6 FET from our inventory. Figure 4-15(a) shows an overall view of this device, and Figure 4-15(b) shows a close-up view of the gate-pad-to-finger transition. The transition over the mesa step is smooth, and no voids were observed in the gate metallization.

It may be that TI received devices from a lot that for their purposes was inadequately screened by the manufacturer. We recommend that the purchaser ask the manufacturer for lot certification of the gate metallization process and that samples of incoming FETs of the Type M-400/6 be subjected to demounting and gate inspection both as received and after a burn-in period under bias.

E2776



(a)



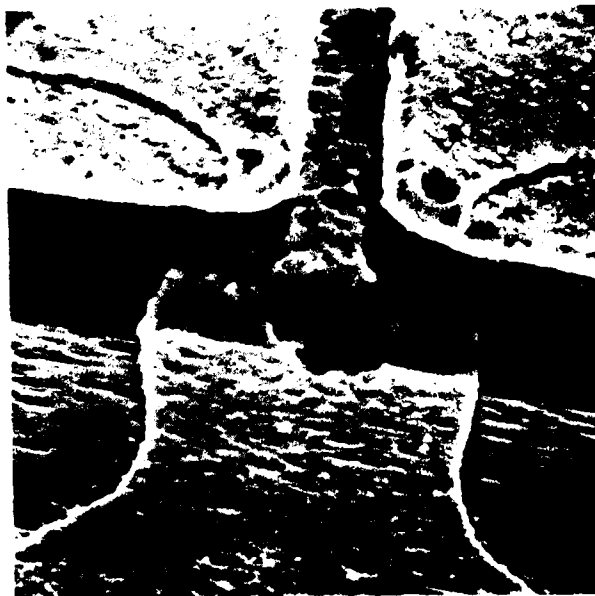
(b)

Figure 4-13 SEM photographs of the Type M-400/6 device. (a) 6000X; (b) 9600X.

E2908



(a)



(b)

Figure 4-14 SEM photographs of the Type M-400/6 14J device. (a) 192X; (b) 6000X.

E2903



(a)



(b)

Figure 4-15 SEM photographs of new Type M-400/6 FET.
(a) Overall view at 195X; (b) Gate
pad to gate finger transition at 7800X.

On the other hand, we note that the manufacturer's maximum recommended operating temperature is far below the temperatures of 185°C and 200°C at which these six Type M-400/6 devices were stressed. If the gate metallization failed as a result of temperature stressing, it could therefore be argued that we have encountered a failure mode that is simply inconsequential at recommended operating temperatures and that extrapolation of observations at 185°C and 200°C to normal operating temperatures is unwarranted. As the intent of accelerated temperature life tests is precisely to be able to extrapolate results to lower, normal operating temperatures, new life test studies would have to be made over a longer period of time at temperatures low enough that the anomaly of the gate metallization failure is insignificant, but still at temperatures sufficiently high that the normal failure mechanism is accelerated. It is important to note that gate metallization deterioration was not observed in Type M-400/6 FETs that failed as a result of deliberate electrical overstressing (Figures 4-5, 4-9, and 4-10(a)).

Still, deterioration of the gate metallization may be the normal failure mode of these lots of this type FET. It should be borne in mind that these FETs were manufactured some two or three years ago. Resolution of so obvious a failure mode as we are discussing here would hardly escape a competent manufacturer's concentrated attention, and, in fact, two papers have recently been presented on gold-metallized gate, medium power FETs^(4,5). Reference 4 discusses a one watt FET similar in many respects to the Type M-400/6 FETs that we have analyzed here. Metal interdiffusion and gold electromigration were clearly evident. On the other hand, Reference 5 reports seeing voiding in an aluminum gate device, but not in a half watt gold gate device, similar to the Type M-400/6, that was subjected to accelerated RF stress testing. We would fully expect to see process improvements to be incorporated into newer devices that would greatly alleviate the sort of metallization problem that we have described here.

We were able to verify through EDAX examination in the voided areas that the underlying refractory Ti-W layer was still present, although miniscule pinholes would have remained undetected. If gold did penetrate to the channel region, the electrical behavior of the FET would, of course, be altered. Additional study effort, perhaps on a subsequent program, would be required to answer additional questions on the failure modes of these Type M-400/6 devices.

4.3.2 Type D-250/6 FETs

Seven failed Type D-250/6 FETs from the TI program were received from RADC for failure analysis. Characteristics of these devices are given in Table 4-5. These are medium power FETs with eight gate fingers, four drain pads, and nine parallel source bonding wires. The devices were fabricated by the LPE technique without a buffer layer and have no n^+ contacts (Reference 2).

SEM photographs of devices #16, #26, and #29 are shown in Figures 4-16, 4-17, and 4-18, respectively. Device #20 was not analyzed, because symptoms of failure were similar to those of device #26.

Figure 4-16(a) shows that the catastrophic failure of device #16 involved a short circuit between a gate finger and the grounded source. Also, there appeared to be some difficulty in attaching the bond wires, and the upper right source bond wire is missing. The normal stitch bond across the four drain pads is also missing. However, the bonding problems do not appear to be implicated directly in the failure of this FET.

Figure 4-16(b) shows a close-up view of the pad end of the gate finger that short circuited. Heat from the large short-circuit current melted the source pad and gate finger. Figure 4-16(b) depicts the radial heat dissipation pattern into the gate pad region. *The similarity of appearance of the failed areas in Figures 4-6 and 4-16 should be noted.*

Figure 4-17(a) shows a SEM photograph of the #26 FET. Note the beautifully cleaved sides of the gallium arsenide substrate, probably the result of a well done scribe and break operation. The wire bonds have a good appearance, and the four drain pads are stitch bonded together. Again, the failure was catastrophic, involving in this device a massive melting of the source, drain, and gate electrodes.

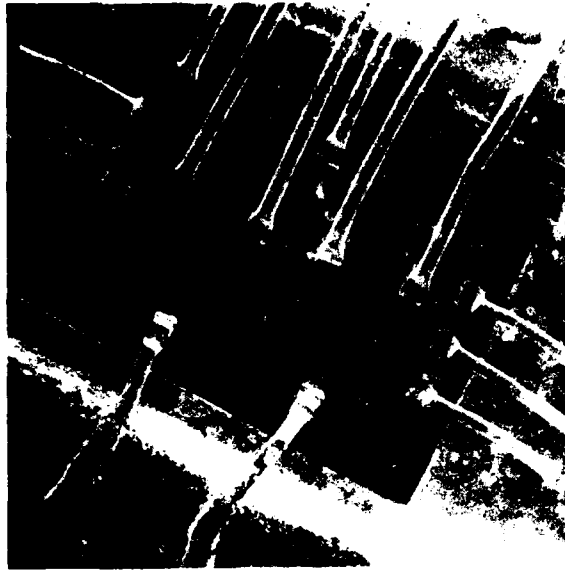
Figure 4-17(b) shows details of the heat flow pattern and the result of resolidification. The failure of this device shows much greater heating than is apparent for device #16 (Figure 4-16). The greater heating possibly was a result of higher short-circuit current that occurred because the failure site was between a drain bond wire and source grounding leads.

TABLE 4-5

CHARACTERISTICS OF FAILED TYPE D-250/6 DEVICES RECEIVED FROM RADC

Device Number	Drain Voltage (V)	Drain Current (mA)	Heatsink Temperature (°C)	Observation
16	8	140	200	Pout was constant until catastrophic failure at 352 hours.
20	8	140	200	Pout was constant for 24 hours and then began to drop. Reached 1 dB down after 42 hours total. Pout continued to drop and device failed catastrophically after 22 more hours.
26	8	140	200	Pout was constant for about 100 hours and then began to drop. Reached 1 dB down after 185 total hours and failed catastrophically shortly afterward.
29	8	140	200	Pout was constant for ~250 hours and then began to drop. Reached 1 dB down after 346 total hours. Ipss was ~20 mA lower.
37	8	125	185	Pout degraded slightly. Testing stopped at 1590 hours. Pout had not degraded 1 dB. Ipss decreased from 385 to 365 mA.
44	8	125	185	Pout degraded 1 dB after 1350 hours. Ipss decreased from 420 to 390 mA.
45	8	125	185	Pout degraded 1 dB after 1500 hours. Ipss decreased from 400 to 370 mA. Gate shorted during attempt to look at reverse I-V characteristic following completion of 1850°C stress test.

E2904



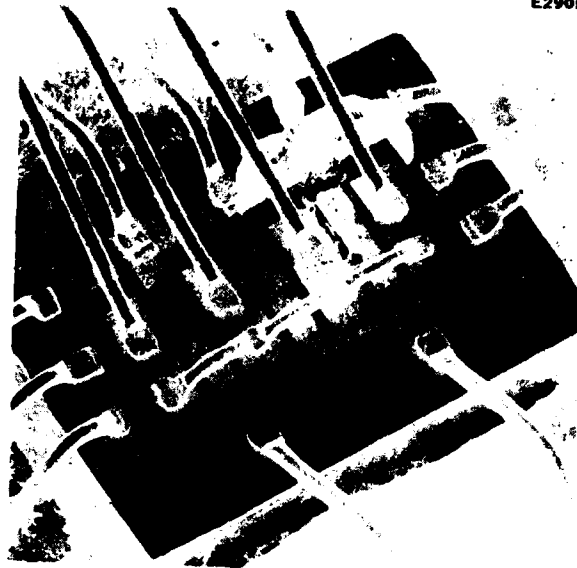
(a)



(b)

Figure 4-16 SEM photographs of the Type D-250/6 #16 FET.
(a) Overall view at 100X; (b) Gate pad to
gate finger transition at 5040X.

E2905



(a)



(b)

Figure 4-17 SEM photographs of the Type D-250/6 #26 FET.
(a) Overall view at 120X; (b) Detail of catastrophic failure showing involvement of source, drain, and gate (270X).

Device #29 degraded in performance and did not fail catastrophically. No indication of the failure mechanism was apparent in SEM photographs. Figure 4-18(a) shows a bubble in the glass passivation, and Figure 4-18(b) shows that a piece of the glass passivation is missing in another region of the FET, but neither problem seems severe, nor would the observed degradation be expected to result from such passivation defects. Deterioration of the metallization or contamination of the channel by impurities diffusing through defects in the glass passivating layer are possible causes of the degradation, but to reach a firm conclusion as to the specific cause of failure would require further study.

Devices #37, #44, and #45 were stressed at 185°C and, as expected, survived considerably longer than the similar devices that were stressed at 200°C. Figures 4-19, 4-20, and 4-21 show SEM photographs of these three FETs. Device #37, shown in Figure 4-19, did not fail. Figure 4-19(a) clearly shows the high quality of die cleavage, mounting, and wire bonding of this FET type. Figure 4-19(b) shows a close-up view of the wire bonds, mesa edge, electrode configuration, and passivating layer.

Device #44 showed gradual degradation of output power until the failure limit of -1 dB was reached at 1350 hours. SEM examination showed an apparent discoloration on the gold surface of the drain pad, located slightly above the arrow in Figure 4-20(a). An EDAX investigation verified that the stain consisted of light elements and hence is surface contamination. Other evidences of contamination are also apparent in Figure 4-20(a). In all likelihood, the foreign matter was not present on the packaged chip, but was introduced during handling procedures after the package had been opened. Thus, the stains played no part in failure of the device.

Figure 4-20(b) is a high magnification picture of a "black spot" in the gold on the drain ohmic contact, identified by the arrow in Figure 4-20(a). Black spots also appear under the gate passivation. These dark areas appear in many SEM pictures of the Type D-250/6 devices. A SEM/EDAX gold mapping of the end of the drain finger showed that the dark areas were sparse in gold, compared to the gold overlay on the drain finger. A SEM/EDAX probe of the dark area in Figure 4-20(b) revealed the presence of gallium, arsenic, nickel, gold, and germanium. Our surmise is that the ohmic contact consists of the popular gold-germanium-nickel-gold combination followed by a gold overlay, and that the dark spots are voids in the surface gold of the contact.

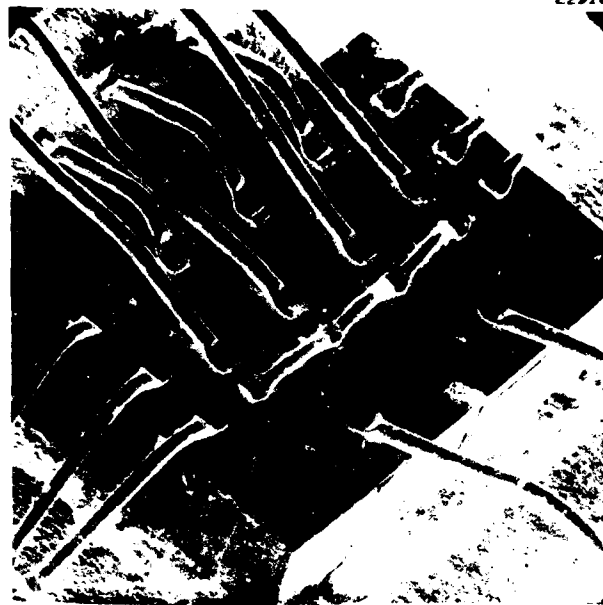


(a)



(b)

Figure 4-18 SEM photographs of Type D-250/6 #29 FET.
 (a) Bubble in glass passivation layer (8400X);
 (b) Piece missing from glass passivation layer (8940X).



(a)

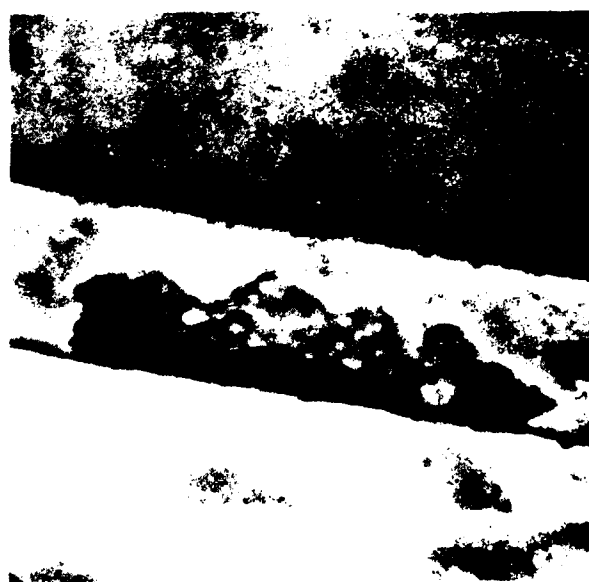


(b)

Figure 4-19 SEM photographs of the Type D-250/6 #37 device. (a) 120X; (b) 800X.



(a)



(b)

Figure 4-20 SEM photographs of the Type D-250/6 #44 device. (a) 165X; (b) 10,800X.

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(a)



(b)

Figure 4-21 SEM photographs of the Type D-250/6 #45 device. (a) 120X; (b) 1200X.

Figure 4-21 shows the #45 FET. Although the device was reported to have a gate-to-source short, no visible evidence of gate failure was found. If the failure was small in extent and located under a stitch bonding wire, it would not be visible in the SEM, however.

Lifting of the side edge of the passivation layer at the side of a central drain pad was observed where the arrow indicates in Figure 4-21(a). Figure 4-21(b) gives a close-up view that indicates a fracture line of the passivation layer at the edge of the gold overlay on the drain pad. However, a slight delamination of the passivation layer would not directly be expected to cause device degradation and failure.

The black spots discussed earlier are again seen in the edge area of the ohmic contact gold. Voids in the gold contact are also in fact present at the edges of the ohmic contact gold under the passivation stripe. However, they are not visible in Figure 4-21(b) because only 5 kV beam voltage on the SEM was used for this picture. A more powerful 20 kV beam makes the voids visible under the glass. Less than optimum ohmic contact metallization may be implicated in the degradation of these devices, but the evidence is not conclusive.

5.0 FAILURE MECHANISM STUDIES

In this section we report our work on investigations of various failure mechanisms in GaAs FETs. The individual projects originated to extend the understanding of device failures that were observed and discussed earlier in this report. These specialized projects are each designed to address specifically a significant potential failure mechanism of major interest in GaAs FET reliability considerations.

5.1 OHMIC CONTACT TESTS

The ohmic contacts have sometimes been implicated in the failure of GaAs FETs. The usual observation is a decrease in current, leading to an assumption of increased resistance in the contacts. However, as discussed in Section 3.5, a decrease in channel doping could also account for this effect.

We set up a test to characterize the failure of the popular Au-Ge/Ni contact made by two different methods. In previous work ("Improved GaAs FET Device," Contract IS-675, COMSAT, July, 1977), we characterized the failure rates of Au-Ge contacts using either Ni or Pt for the high temperature metal "cap". We found little difference between them to first order. The present experiment gives us an opportunity to compare two, somewhat different, ways of preparing the popular alloyed Au-Ge/Ni contact. Table 5-1 gives the pertinent data on the contacts. The "thick" metal contact has a different choice of thicknesses for the metal layers and is also alloyed at a different temperature from the "thin" metal contact.

The structures being tested are complete FETs made by Hughes in which the aluminum gate electrode is not wire-bonded. All the channels are silicon implanted into bulk-grown substrate wafers. The initial sheet resistivity is about 300 ohms/square. The devices are divided into groups of 5, and a biased and an unbiased group of each metal type was tested at three temperatures, 12 groups in all. The drain current at temperature is 10 mA at whatever voltage is required to maintain that current; however, the voltage in every case is below the saturation voltage for these 300 μ m gate width FETs. To determine the drain-source resistance, R_{DS} , we first brought the devices back to room temperature. The drain current at a voltage of 0.5 volts was then measured, and R_{DS} was determined.

TABLE 5-1
OHMIC CONTACT PROCESS PARAMETERS

Parameter	Thick	Thin
Au-Ge, Å	1500	750
Ni, Å	400	150
Au, Å	500	1200
Alloy Temp., °C	480	360
Alloy Time, sec.	60	60

Figures 5-1 and 5-2 show the behavior of R_{DS} with time. As we see, the annealing behaviors of the two types of alloyed contacts are remarkably similar. There are no systematic differences between biased or unbiased, thick or thin contacts. In several of the plots there is an initial increase of R_{DS} on heating. R_{DS} soon stabilizes, however, and there is no further change out to some 1000 hours, even at 260°C. Consequently, our recommendation is that all devices be subjected to an initial burn-in period without bias.

These data indicate that the life of ohmic contacts made by either method is at least several times higher than that of the rest of the FET, neglecting the initial change. Therefore, process variations may have minimal effects on contact reliability. However, each contact process tested here was initially optimized for low resistance. Thus, we cannot conclude that all variations in metallization will result in acceptable lifetimes.

5.2 GOLD GATE RELIABILITY

We made a few isolated tests on medium power FETs to determine the reliability of the gold-based gate metal diode. In Section 3.5 above, we reported the failure of the gold gate Type A-6 low noise FETs, apparently due to changes in channel doping. Even though we carried those tests at 260°C out to over 500 hours, there was no instance out of 15 FETs of the gate current increasing. This observation about the Type A-6 FETs at 260°C was also true for temperatures of 200°C and 240°C, where times exceeded 1000 hours. We concluded that the gate diode did not degrade on the Type A-6 FETs.

The power FET type that we tested will be termed T-1000/10. It has a Ti-Pt-Au metallization, based on vendor comments. We stored the devices at 260°C without bias in dry nitrogen. Measurements were made using a Tektronix 576 curve tracer. The results are shown in Table 5-2. Clearly, this gate diode degrades with temperature. Cell B of Chip #1 failed on testing, perhaps due to poor test technique. Cell A of Chip #1 failed at 16 hours, 260°C. Cell A of Chip #2 held up well.

These devices are made using a lift-off process, with sequential evaporations of Ti-Pt-Au. This process is different from that of Vendor A, at least in the choice of refractory metal. Vendor A's was Ti-W.

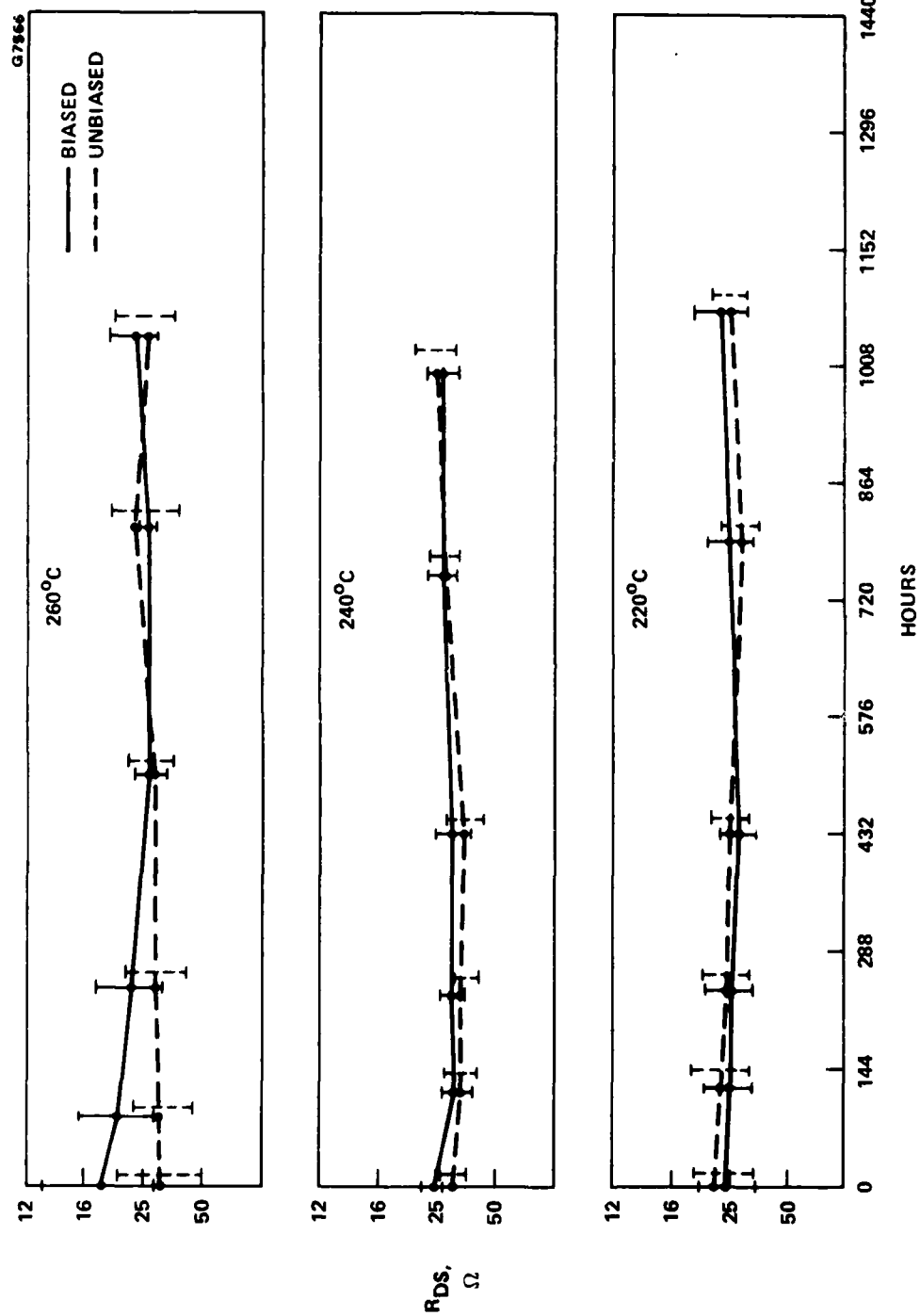


Figure 5-1 Change of ohmic contact resistance upon heating for thick Au-Ge/Ni ohmic contact alloyed at 480°C. Biased samples are held at 10 mA. The horizontal bars indicate ± 1 standard deviation in current at a measurement voltage of 0.5 volts. For clarity the bars on unbiased device measurements have been offset to the right. Note inverted ordinate scale.

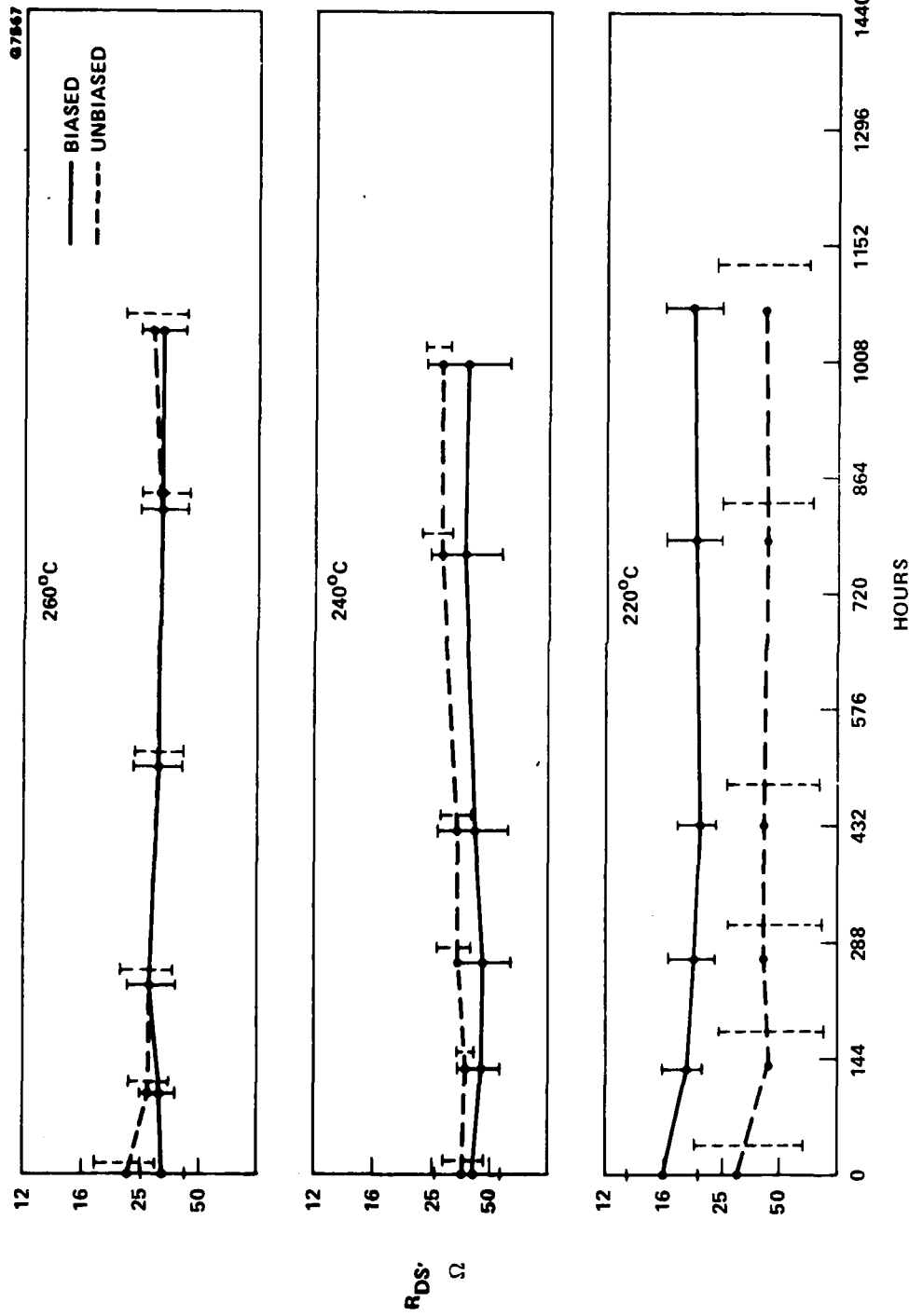


Figure 5-2 Change of ohmic contact resistance upon heating for thin Au-Ce/Ni ohmic contact allowed at approximately 360°C. Biased samples are held at 10 mA. The horizontal bars indicate ± 1 standard deviation in current at a measurement voltage of 0.5 volts. For clarity the bars on unbiased device measurements have been offset to the right. Note inverted ordinate scale.

TABLE 5-2
GATE DIODE DEGRADATION AT 260°C, TYPE T-1000/10 FET

Time, Hr.	Temp., °C	CHIP #1		CHIP #2	
		Cell A μA/V	Cell B μA/V	Cell A μA/V	Cell B μA/V
Before Mounting		2/2.7	2/2.8	2/4.3	2/4.3
<0.1	280-300	2/2.7	2/2.3	2/4.2	No test
2	260	--	2/2.5	2/4.2	
6	260	--	--	2/4.1	
16	260	5/0.6 20/1.7	--		
22	260	--	--	2/3.2	
88	260	5/0.2 20/0.35		2/2.8	
286	260	20/0.2 100/0.8		2/2.2	

Note: The temperature of 280-300°C shown above was encountered only during die mounting and wire bonding.

We want to point out the importance of testing specific devices from a given vendor's lot, even when it seems to be similar to that of others. The reliability of gate electrodes in FETs has frequently been simplified to gold versus aluminum. However, based on the data we have seen so far, the Ti-W-Au gate of Type A-6 FETs is among the most reliable, maybe better than the Al gate as far as the gate diode quality is concerned. This observation leaves aside the questions of gate current and electromigration. However, the gate diode of the T-1000/10 FET that we tested was marginal, even though made using a refractory-gold composite.

We are of the opinion that the refractory-gold processes are inherently more difficult to perfect than aluminum processes. The gold process also may be more difficult to control. However, there is much more to learn about the gold versus aluminum question. For low noise FETs the question may be academic, because high reliability FETs with excellent performance are being built with either gold or aluminum gates. The issue requires more study in the case of power FETs.

5.3 GOLD-ALUMINUM CONNECTORS

In the fabrication process of making aluminum gates, typically gold pads are used for external wire bonding. The gold and aluminum must be separated by a refractory metal interface to prevent the formation of the undesirable intermetallic compound known as "purple plague." One of the tests that we have carried out in our investigations of the basic failure mechanisms of GaAs FET technology is related to possible defects in the construction of Au-Al connectors in FETs with Al gates.

Two basically different constructions are used, as shown in Figure 5-3. In Figure 5-3(a) the Au overlays the Al in the wire bond area. This pad design is subject to penetration of the refractory metal barrier by the bond force, so that the Au-Al purple plague can form. In Figure 5-3(b) such penetration cannot occur, if bond placement is correct. Therefore, the bonded contact is subject to inspection and screening. Wafer qualification can determine if the refractory metal barrier is reliable.

However, inspection of Figure 5-3(b) reveals other possible defects. As drawn, the figure shows Au overlaying the Al and climbing over its edge. The refractory is thin at this point and subject to the usual cracks and defects that result from applying a thin

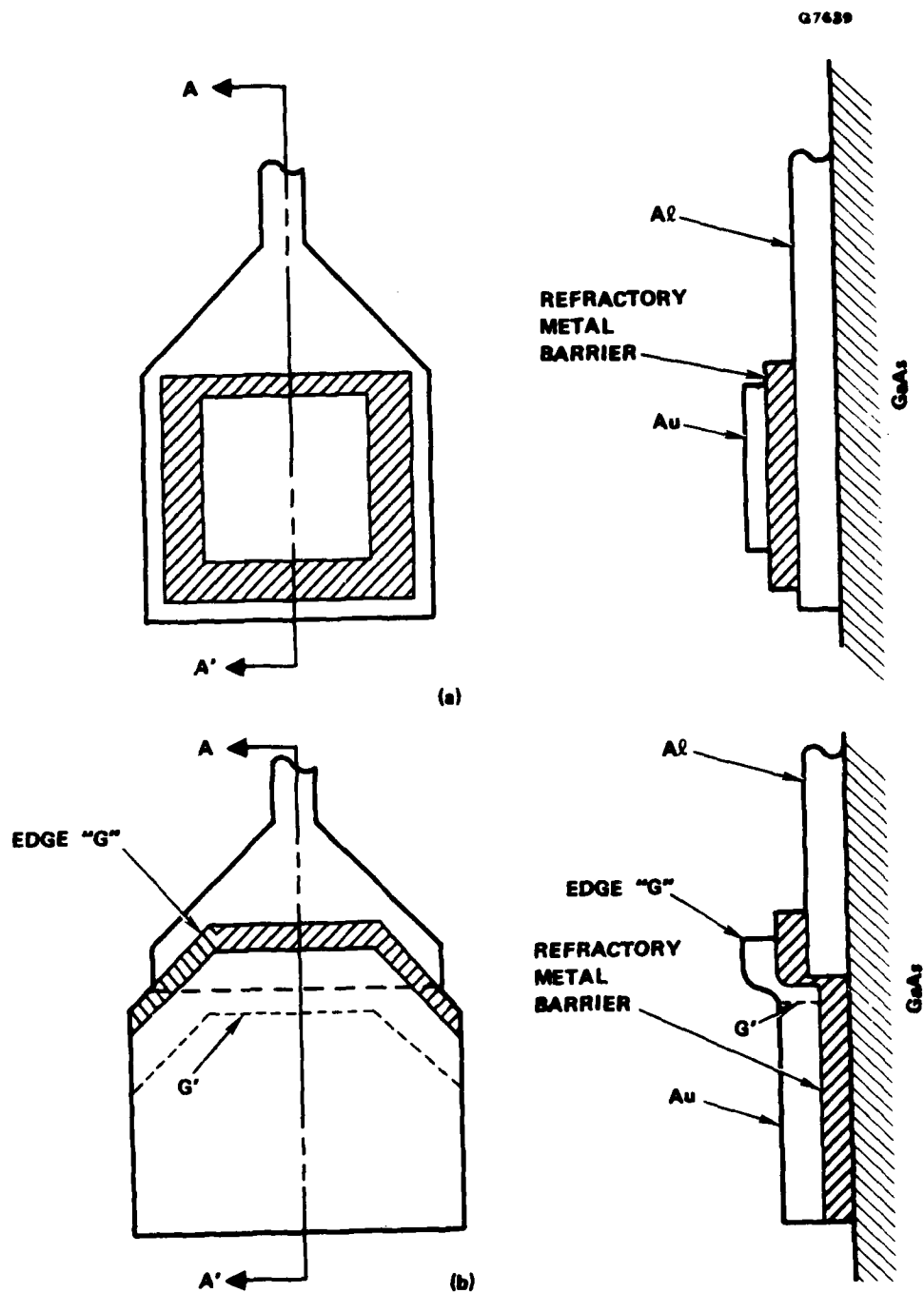


Figure 5-3 Gate connector designs, gold-aluminum. (a) Gold overlays Al in band area. (b) Gold does not overlay Al in band area. See text for details.

metallization layer over an abrupt step. An alternative is to remove the gold edge back to the point labeled "Edge G'," so that the Au cannot possibly penetrate the refractory to the aluminum.

Examples of these situations are found in current practice. Type H-1 low noise FETs have the Figure 5-3(a) pad design, and Type N-2 FETs have the Figure 5-3(b) design with "Edge G." Type N-3 FETs have the Figure 5-3(b) "Edge G' " design.

We have carried out a test of the Figure 5-3(a) design using type H-1 low noise FETs. The purpose of the test was to investigate the effects on reliability of (a) defects resulting from probe marks, and (b) wedge bonding forces.

Five Type H-1 unpackaged devices were investigated to determine possible gate contact degradation due to application of excessive wedge force during the bonding operation. Four of the five devices had marks on the gate pad, apparently from having been previously tested by the vendor. The aluminum gate pad has a Cr-Pt-Au overlay, and it is the gold-aluminum proximity that was studied for possible atom migration and formation of intermediate compounds. The following test conditions were established:

FET A: A heavy wedge force of 40-42 grams was applied to the gate pad. The force was considerably above the force that would be used in a normal bonding operation, and the gate pad therefore was damaged as intended. The aluminum under-layer was exposed in the wedge region.

FET B: Superficial testing marks were observed on the gate pad. This FET was put on test to determine the behavior of a normal device.

FET C: The gate pad on this device showed no evidence of having been contacted previously. A normal wedge force of 20-22 grams was applied, creating visible indentation marks in the gold, but no observable penetration of the gold to the underlying metals.

FET D: This FET had a testing mark at the edge of the gate pad, apparently extending across all three gate metals. A normal force of 20-22 grams was applied to the wedge, which crossed all three gate metals on the opposite side of the testing mark.

FET E: On this device the gate pad has a deep wedge mark due to vendor probing that extends into the aluminum layer, similar to the situation of the gate pad on FET A that was intentionally damaged.

A summary of the initial test conditions is given in the first three columns of Table 5-3. The fourth column of Table 5-3 refers to the particular figure number corresponding to the test in question. Figures 5-4 through 5-9 show photographs of the gate pads before and after high temperature storage.

The five chip devices were stored at 260°C in a dry N₂ gas atmosphere and were observed at periods of 312, 487, and 576 hours, cumulative. The test was discontinued at 576 hours total time. Gross degradation of the gate pad and gate feed areas had occurred even prior to the first observation at 312 hours. Small additional changes were noted in these areas as the time of storage at temperature progressed to the termination time.

Figures 5-4 through 5-9 clearly show the migration of aluminum into the gold. We also observe that formation of the intermetallic compound occurred in more widespread areas than the wedge marks encompassed.

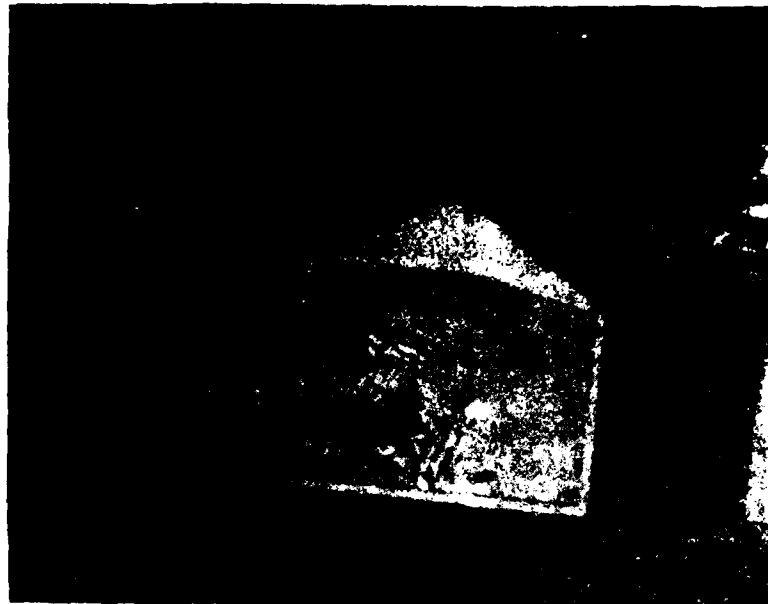
Figure 5-6 (Device B) indicates that, in addition to the intermetallic formation, a delamination of the glass over the gate area also occurred during high temperature storage. This phenomenon was absent in the remaining four devices. All devices, however, exhibited gross intermetallic growth. In each case it was initiated at the metallization defects. Note also that the Au-Al intermetallic growth is always associated with the mottling of the Al metallization. This mottling results from Al migration into the Au gate pad, as confirmed by EDAX scans.

After high temperature storage, in addition to severe degradation of the gate contact, noticeable mottling was observed on the source and drain contacts. This effect can be seen clearly in Figures 5-8 and 5-9. As the high temperature storage test progressed, I_{DSS} values were monitored and found to decrease progressively as the mottling of the source and drain pads visually increased, indicating increased ohmic contact resistance. The five unpackaged chip devices were initially processed onto 1 cm by 1 cm alumina microstrip substrate carriers with Au-Sn eutectic solder and then source/drain bonded using 0.7 mil half-hard gold wire. Photographs and I_{DSS} measurements were

TABLE 5-3

TYPE H-1 FET: UNBIASED DEVICE STORAGE AT 260°C

Device	Initial Gate Pad Characterization	Disturbance	Figure Number	I_{DSS} , mA, at $V_{DS} = 1.5V$		
				Initial	487 Hrs	576 Hrs
A	Light vendor testing artifact	Hughes 40/42g wedge force over artifact	5-4	70	45	30
B	Light vendor testing artifact	No disturbance	5-5 and 5-6	78	48	37
C	No vendor testing artifact	Hughes 20/22g wedge force	5-7	79	50	27
D	Vendor testing artifact across edge of Au/Al pad	Hughes 20/22g wedge force across opposite pad edge	5-8	76	48	30
E	Deep vendor testing artifact	No disturbance	5-9	58	33	27



(a)



(b)

Figure 5-4 Type H-1 FET, same A. (a) After 40/42g wedge force. (b) After 312 hours storage at 260°C. 500X magnification.

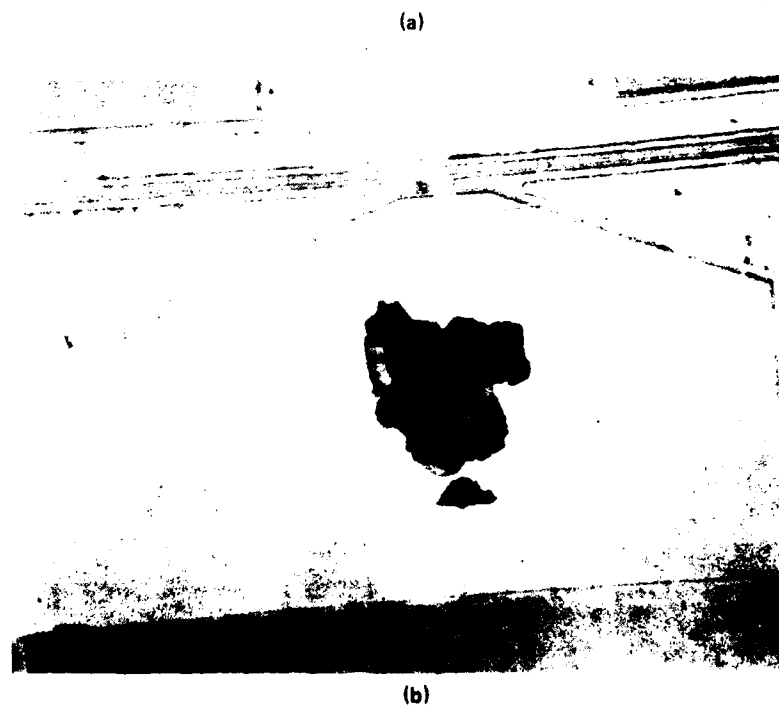
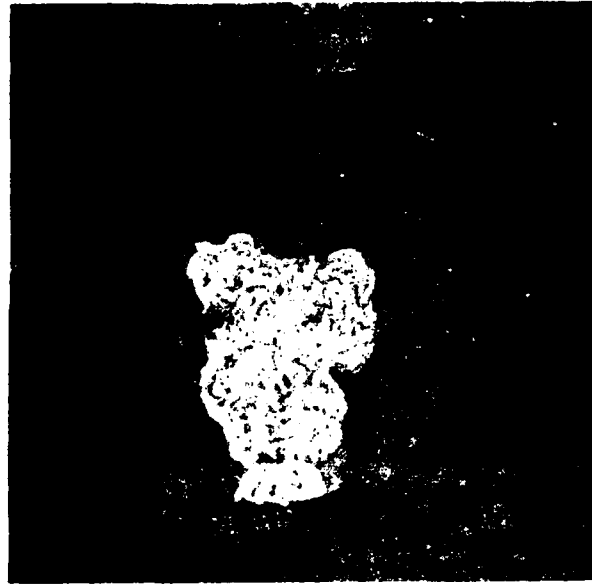


Figure 5-5 Type H-1, sample B. (a) Initial appearance, 500X. (b) After 312 hours at 260°C. 500X magnification.

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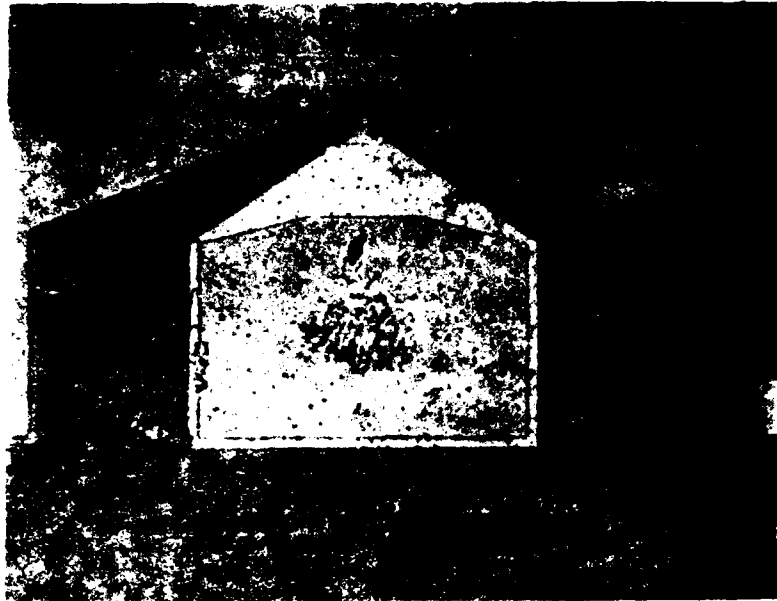


(a)



(b)

Figure 5-6 Type R-1 Zn, sample C, after 576 hours at 2600C in N₂ gas. Intermetallic growth resulting from a testing artifact. (a) optical photograph at 600X; (b) SEM photograph at 100X.

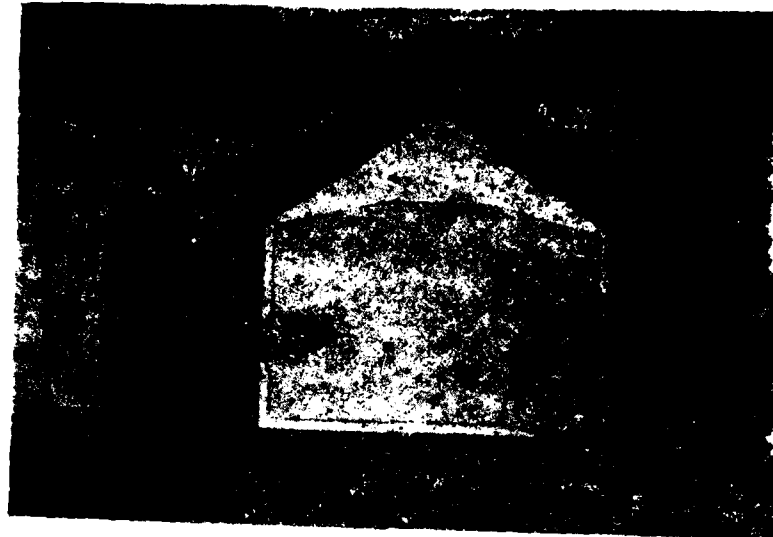


(a)

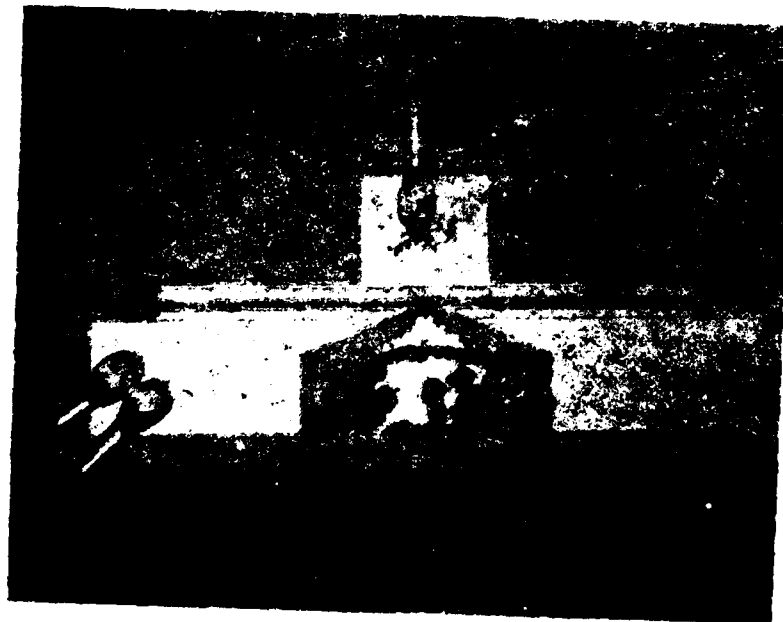


(b)

Figure 5-7 Type B-1 FET, Sample C. (a) After 20/22g normal wedge force. (b) After 312 hours at 260°C, 500X magnification.

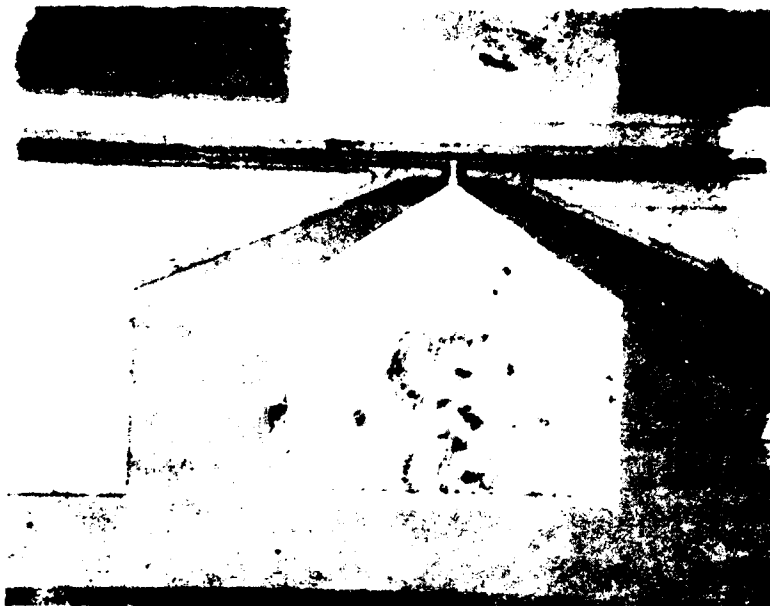


(a)

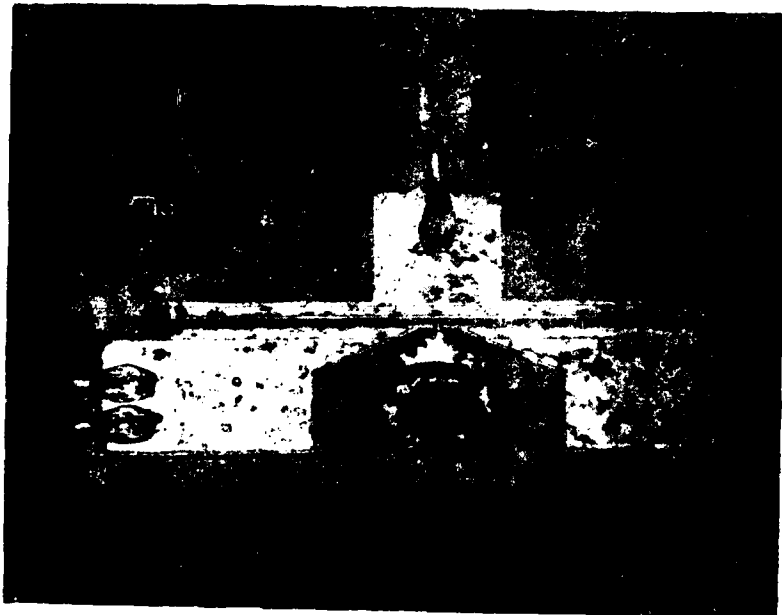


(b)

Figure 5-8 Image 4-1-10, Sample 0. (a) After 20/22g with 1.5 hr. of contact. Other defect in visible area. (b) After 312 with 1.5 hr. of contact. No visible contact notches apparent.



(a)



(b)

Figure 5-9 Type H-1 FET, sample E. (a) As received condition. 500X. (b) After 312 hours at 260°C. Note mottled source and drain areas. 200X.

made prior to and at measurement times during elevated temperature storage. Results of the I_{DSS} measurements are summarized in the last three columns of Table 5-3.

Though the amount of intermetallic compound that formed in the gate pad area is large in all cases, it was usually more localized in the initial defect areas. In Figure 5-7, Sample C, however, the effect is more general, suggesting a more basic process problem.

Device failures from the high temperature stress tests that may involve the formation of Au-Al intermetallic compounds are discussed in Section 3.6. We conclude that the type of bond pad shown in Figure 5-3(a) is probably not as reliable as that shown in Figure 5-3(b). In Figure 5-3(a) great care is needed to avoid puncture of the refractory metal barrier. Excessive bond wedge force is difficult to detect, and damage to the pad can easily be covered up by a subsequent bond.

Finally, it is most important to recognize that, although these tests illustrate the formation of "purple plague" in Type H-1 FETs, the type H-1 FET is obsolete and is no longer being supplied by the manufacturer. We recommend strongly that the user perform his own reliability tests on devices presently being supplied, in cooperation with the manufacturer.

5.4 RESISTANCE OF GOLD PAD - ALUMINUM GATE TRANSITION

Aluminum is known to undergo changes in grain structure as a result of thermal cycling. The grains grow larger, and the surface of an otherwise smooth aluminum layer in the 0.5 μm thickness range becomes much more rough-looking. Increases in resistance can occur. Also, the gold gate pad transition to the aluminum gate may undergo changes in resistance more subtle than the effects discussed in Section 5.3.

To get data on this range of effects we have measured the resistance of an aluminum, low noise FET gate electrode as a function of time at high temperature storage. The FET has an aluminum gate electrode that has a true 0.5 μm gate length and about 0.4 μm thickness. The gate transition design is essentially the same as that of the Type N-3 low noise FET or of the Type N-200/6. For the device that we tested the refractory metal is a Ti-Pd combination.

We will designate the FET as a Type E-10. An optical photograph of the device as it was bonded for this test is shown in Figure 5-10. The bond wires are positioned to attach to two separate circuits so that the current between the two gate pads can be measured. As this system is ohmic, for fixed applied voltage the series resistance is inversely proportional to the current.

Figure 5-11 charts the measured current with 50 mW applied between the two pads, with heating time as the abscissa. No voltage was applied during heating. For the 200°C test only 3 devices were tested, and at 260°C 10 devices were tested. At 200°C one of the devices was an open circuit after 184 hours, and at 260°C, one device opened after 286 hours. Examination of the two failed devices showed in each case that a gate wire had become detached from the carrier. These failures were mechanically induced in handling and are therefore censored from the analysis of the results.

The plots of Figure 5-11 show an initial decrease in resistance by a factor of 3 during the first hours. Had we measured the 260°C batch over shorter intervals, we probably would have found a shorter transition to low resistance than at 200°C. Note that studies of the ohmic contact resistance, Figures 5-1 and 5-2, show an initial increase of resistance. Our recommendation again is that devices be given an initial burn-in period.

A careful look at the 260°C curve in Figure 5-11 beyond 288 hours indicates that the long term trend is for a slow increase in resistance. We do not know if this is due to the Al gate or to the transitions. We believe that the initial change is due to lower resistance in the refractory metal interface. Both test groups approach 31 ohms as an asymptote, and this value is close to the computed value for the Al gate stripe.

The data at 260°C indicate that changes in the resistance of the Al stripe are probably not a factor in device degradation in high temperature stress tests on low noise FETs. The curves of Figure 5-11 also reveal a possible solution for the rapid initial change in device parameters that is sometimes seen in life testing. In the Au-Al gate pad-gate electrode technology, annealing of the device may be needed to stabilize it. Of course, the metallization investigated here is different from that of other vendors, and each case should be treated uniquely.

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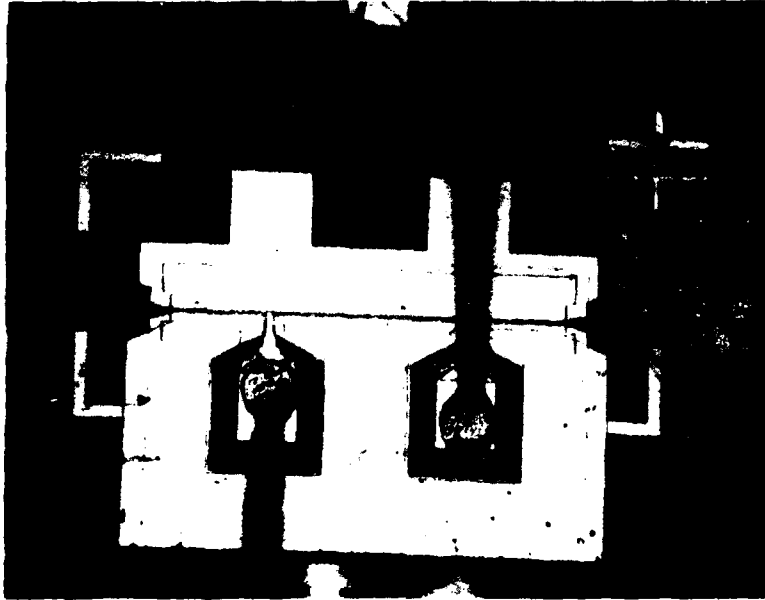


Figure 5-10 FET type E-10 bonded for gate-to-gate resistance tests.

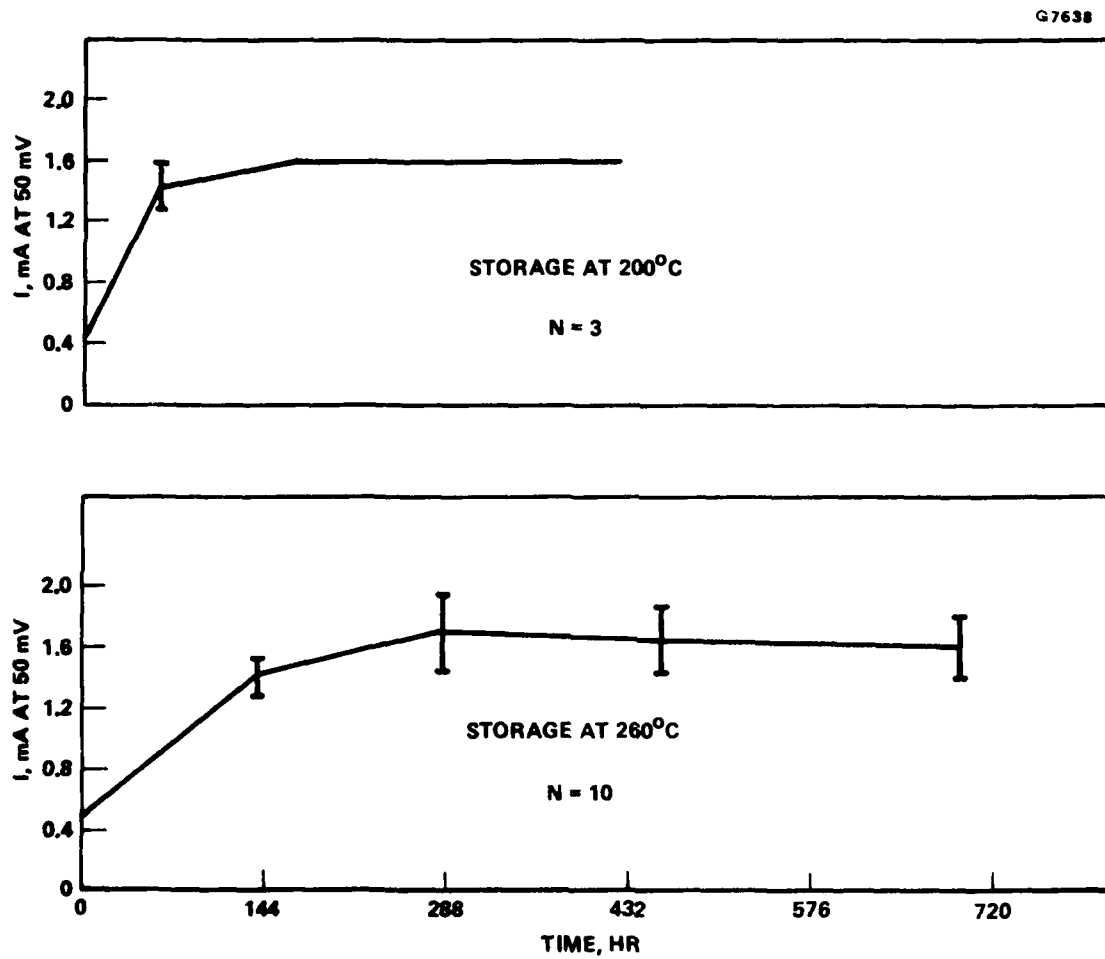


Figure 5-11 Current at 50 mV through a 0.5 μ m gate stripe heated without bias at 200°C and 260°C. N = number of devices starting the test. The horizontal bars indicate ± 1 standard deviation.

6.0 SUMMARY

In this report we have discussed the characterization of the power FETs procured for this program and failure analysis of low noise devices, including wire bonding failures and environmental stress test failures. A method of etching gold while leaving the underlying refractory metals relatively unaffected was explained. An analysis of the Type A-6 low noise FET was given, in which a failure mode was discussed that involved possible channel doping compensation. Results were then presented on device failures from high and medium temperature stress tests on low noise FETs.

A number of medium power devices were received from RADC for analysis. These were packaged FETs that had been subjected to various stresses at Texas Instruments on a RADC/TI reliability contract. Typically, the devices had failed during deliberate stressing to the *maximum* electrical limits or in temperature stress tests.

Failure mechanism studies of two different ohmic contact metallizations showed that both fabrication procedures produced reliable contacts. Constant elevated temperature tests of gold-based gate diode FETs from two different manufacturers showed that one device type was considerably less prone to gate diode failure than the other, indicating the necessity of additional work on the gold gate versus aluminum gate reliability question.

Failures were investigated that involve problems associated with gold contact pads overlaying aluminum gate pads with a refractory metal interface. Finally, temperature-accelerated studies of the resistance of aluminum gates were carried out.

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APPENDIX A

RECENT RESULTS OF FAILURE ANALYSIS OBTAINED AFTER PREPARATION OF THE FINAL REPORT DRAFT

An addendum to the term of the contract was arranged to present failure data obtained after the final report draft on this program had been submitted. The additional information was obtained through November 1980. Failure analysis is given on devices obtained from the medium temperature constant stress tests and the RF constant stress test of the RADC/Hughes Low Noise FET Reliability Program.⁽¹⁾ Failure analysis is then given on devices recently provided by RADC from the RADC/TI Medium Power FET Reliability Program.⁽²⁾

A.1 RADC/HUGHES LOW NOISE FET RELIABILITY PROGRAM

A summary of recently obtained reliability information on low noise FETs is given in Appendix B of Reference 1. Two constant temperatures, 85°C and 120°C, were used to stress low noise packaged FETs. Another group of packaged FETs was stressed at 200°C under low noise DC bias in an RF amplifier configuration. Results of failure analysis on devices from these tests are given below.

A.1.1 Medium Temperature Constant Stress Tests

A.1.1.1 Packaged FETs stressed at 85°C - A summary of the status of packaged devices for the 85°C constant stress test is given in Table A-1, which is taken from Table B-1 of Reference 1. A representative selection of 11 devices out of 28 was taken, and these FETs were analyzed. Included in the sample are temperature-related catastrophic gate and source failures, degradation failures of drain current, and for comparison some devices that did not fail. Each device type in the test is represented.

Table A-2, which is taken from Table B-2 of Reference 1, shows a matrix of the categories of failures in the 85°C stress test. An asterisk indicates that one or two devices from that category were selected for failure analysis. As part of the analysis

TABLE A-1
FAILURE ANALYSIS OF PACKAGED DEVICES FROM 85°C CONSTANT STRESS TEST

Serial Number	Type Code	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Related Failure	Other Failures	Figure Number
3	R-51	U		3,931	Open source		A-10
6	H-21	B		1,457	I _{DSS}		
7	H-21	B		331	I _{DSS}		A-5
8-A	H-21	B		331	I _{DSS}		
8-B†	D-11	B		1,764	G/S Short		A-2
9-A	H-21	B		331	I _{DS}		
9-B	D-22	U		1,457	I _{DSS}		
10	H-21	U		1,764	Gate Control		A-4
12	A-51	B		3,931	Gate Control		A-1
13	A-51	B		3,148	I _{DS}		
16	A-51	B		0		Set up	
17	N-21	U		1,457	I _{DSS}		A-6(a)
19	N-21	U		1,457	I _{DSS}		
20	N-21	B	4,221				A-6(b)
21-A	A-51	U		0		Set up	
21-B	H-1A1	B		1,457	I _{DS}		
22	H-1A1	B		1,764		Lost	
23-A	H-1A1	U		1,457	I _{DS}		A-3
23-B	N-32	U	4,221				A-8
26	N-32	U		1,457	I _{DSS}		A-9
30	H-1A1	U		1,457	I _{DS}		
34-A	N-32	B	4,221				
34-B	A-51	B		1,457		Set up	
41	N-31	B		1,457	I _{DS}		
42	N-31	B	4,221				
44	N-31	B	4,221				
73	N-31	U		1,764	G/S Short		A-7
93	N-31	U		3,931	I _{DSS}		

†Note: Device #8-B was carried in inventory as a Type D-22 FET. See text.

TABLE A-2
CATEGORIES OF FAILURES IN 85°C CONSTANT STRESS
TESTS ON PACKAGED DEVICES

Type Code	No. FETs Started		Not Failed		Set-Up Failures		Related to Temperature						Figure Numbers		
							Temper- ature Failures		Gate Control		Gate Short			Open Source	
	B	U	B	U	B	U	B	U	B	U	B	U		B	U
A-51	4	1			2	1	2		1*					1	A-1
D-11	1						1								
D-22		1					1			1*				1	A-3
H-1A1	2	2		1			1	2						1*	
H-21	4	1					4	1		1*				4*	A-6
N-21	1	2						2						2	
N-31	3	2					1	2			1*			1	A-8, A-9
N-32	1	2		1*				1						1*	
R-51		1						1					1*		
Totals	16	12	4	1	3	1	9	10	1	1	1	1	1	7	

*Discussed in the text

procedure, the packaged FETs were delidded and SEM photographs were taken of the chip. Figure numbers corresponding to the SEM photographs are given in the right hand column of Tables A-1 and A-2. Observations and comments on the failures follow. The order of presentation is alphabetical by Type Code.

Figure A-1(a) shows a Type A-51 FET that was listed as a failure after 3,931 hours at 85°C when the gate bias no longer controlled the drain current. Figure A-1(b) shows the source, drain and gate electrodes melted together and a crack in the gallium arsenide. The crack probably occurred when the package was delidded and is not part of the failure mechanism.

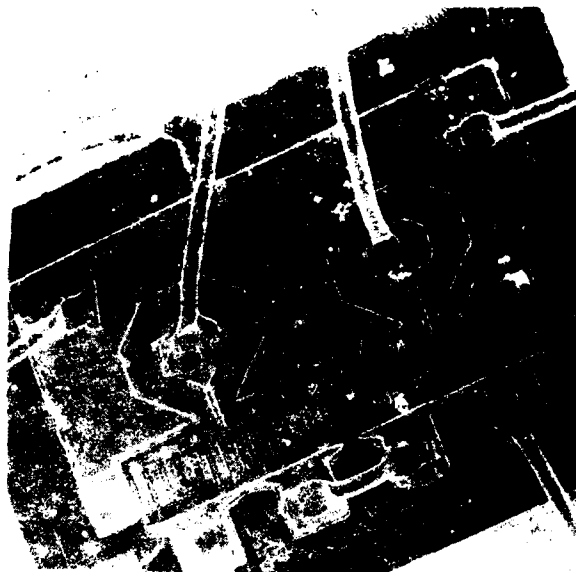
The device shown in Figure A-2 failed with a gate-to-source short circuit at 1,764 hours. The device has been carried in inventory and throughout the 85°C tests as a Type D-22 FET. When the package was delidded, however, to our surprise the FET was Type D-11. Massive melting of both gate pad regions is shown in the figure.

The Type H-1A1 FET illustrated in Figure A-3 showed a decrease in drain current. Mottling of the ohmic contact metallization can be observed, as well as some spotting of the aluminum gate pad transition.

Figures A-4 and A-5 show two Type H-21 FETs from the same manufacturer as the Type H-1A1 devices. Again, mottling of the ohmic contact metallization is apparent. The edge of the aluminum gate transition is ragged.

Two Type N-21 FETs are shown in Figure A-6. Fabrication of the mesa step, the metallizations, the wire bonding, and the general appearance of this FET type are clearly superior. As all devices in the "Not Failed" column of Table A-2 were FETs from manufacturer N, we also conclude that Type N devices are highly reliable.

When Type N devices do fail, the failure site typically is localized near the gate-pad-to-finger junction. Figure A-7 shows a Type N-31 FET that failed after 1,764 hours at 85°C with a gate-to-source short circuit. The Type N-32 FET is the same chip type as the Type N-31 FET, but in a different package. After 4,221 hours at 85°C the Type N-32 FET shown in Figure A-8 had not failed. Figure A-9 depicts a Type N-32 FET that failed near the gate-pad-to-finger junction.



(a)



(b)

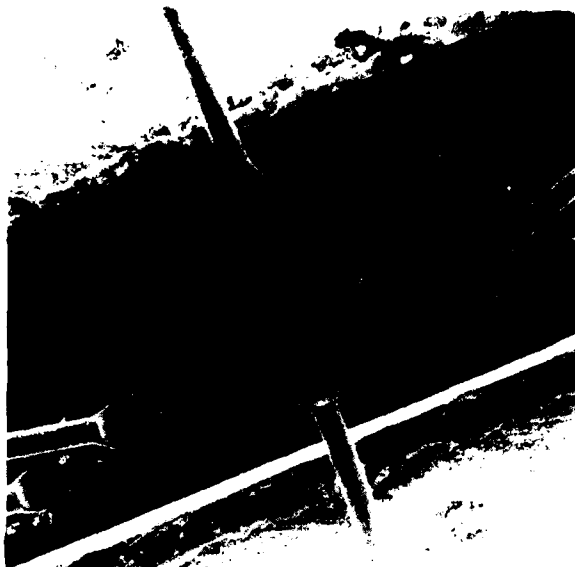
Figure A-1 Type A-51 #12 FET. Note
two failure sites. (a) 160X.
(b) 1700X.

E3032



Figure A-2 Type D-11 #8-B FET that failed with a gate-to-source short circuit. 200X.

E3033

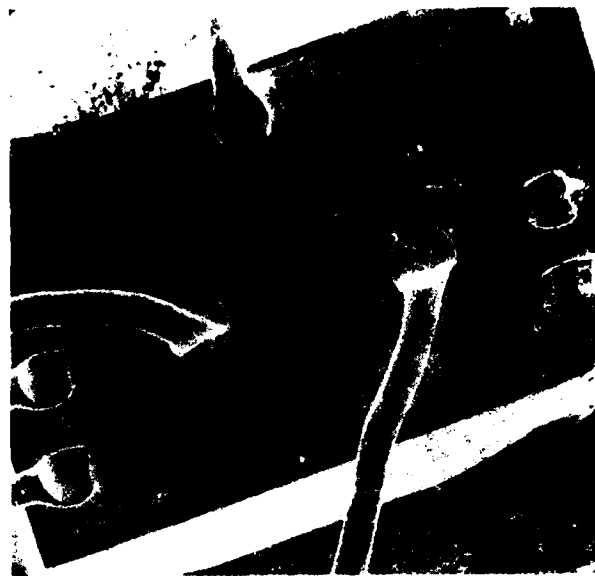


(a)



(b)

Figure A-3 Type H-1A1 #23-A FET that showed a decrease in drain current.
(a) 150X. (b) 1500X.



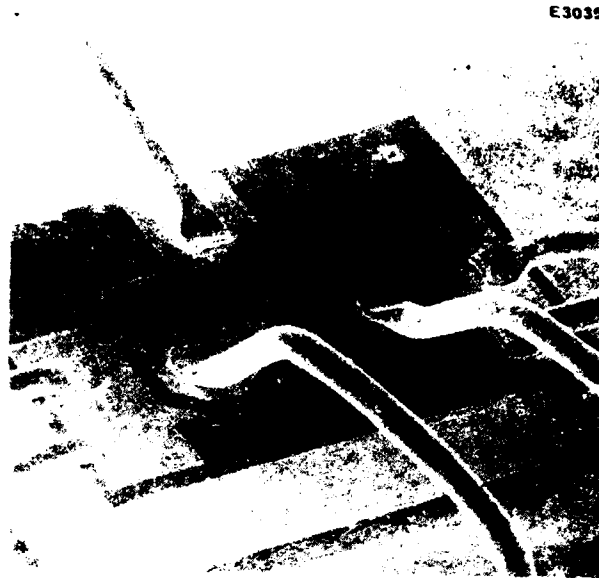
(a)



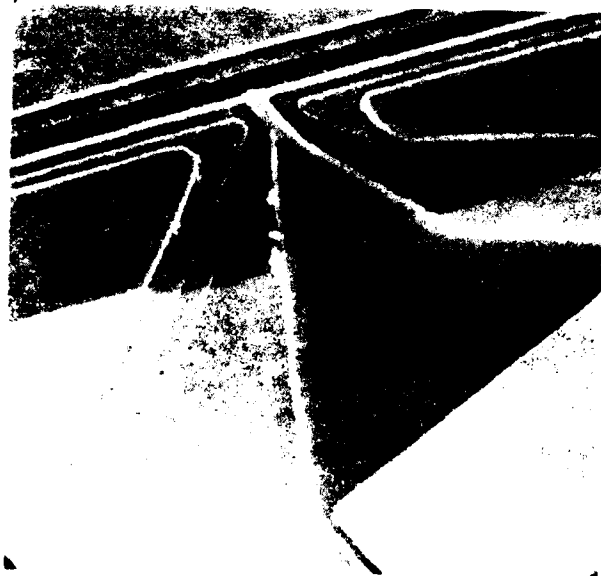
(b)

Figure A-4 Type B-21 #10 FET that lost gate control (a) 30X. (b) 4480X.

E3035



(a)



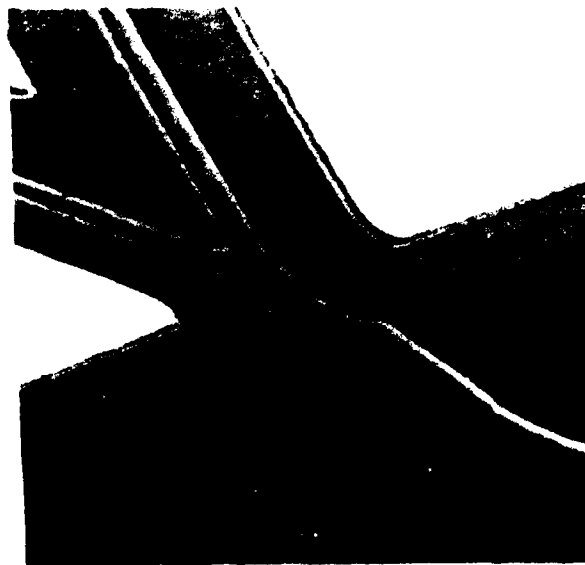
(b)

Figure A-5 Type H-21 #7 FET that showed a decrease in saturated drain current. (a) 160X. (b) 1600X.

E3036



(a)



(b)

Figure A-6 Type N-21 FET. (a) #17 that showed a decrease in I_{DSS} . 230X.
(b) #20 that did not fail. 2400X view of gate terminus.



Figure A-7 Type N-31 #73 FET that failed with a gate-to-source short circuit at the left gate pad connector. 2400X. An overall view of a similar chip is shown in Figure A-8(a).



(a)



(b)

Figure A-8 Type N-1 8.5-B FET that did not fail. (a) 100X. (b) Close-up view of right gate pad connector, 1040X.

E3039

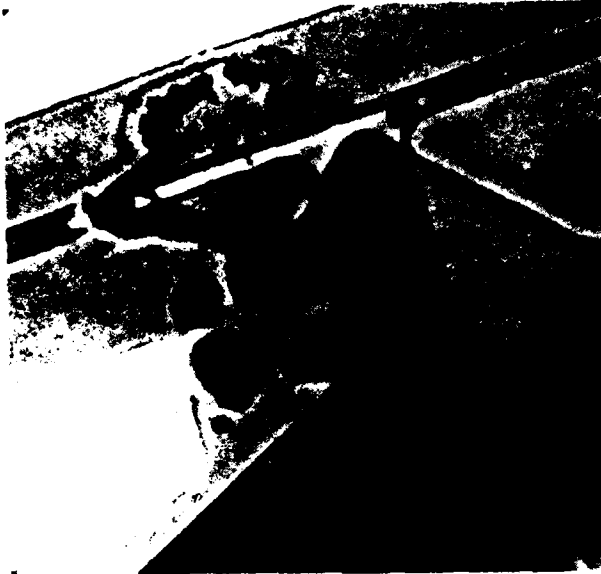


Figure A-9 Type N-32 #26 FET that showed
a decrease in I_{DSS} . Close-up
view of left gate pad connector.
2600X.

The only source failure in the medium temperature tests was of a Type R-51 FET, shown in Figure A-10. The now-familiar corrosion of the source lead depicted in Figure 3-4 can be observed in Figure A-10. It is unfortunate that the shipment of Type R-51 FETs that we received characteristically exhibited the source lead corrosion problem. Manufacturer R is a highly competent firm with an enviable record of superior work, and these Type R-51 FETs are simply not representative of his products.

A.1.1.2 Packaged FETs stressed at 120°C - A summary of the status of packaged devices for the 120°C constant stress test is given in Table A-3, which is taken from Table B-3 of Reference 1. A representative selection of 9 devices out of 26 was taken, and these FETs were analyzed. Included in the sample are temperature-related catastrophic gate short failures, degradation failures of drain current, and for comparison some devices that did not fail. Each device type that had temperature-related failures is represented. For the failure analysis work presented here, device selection from the 120°C test was correlated with device selection from the 85°C test to give broad coverage of failure modes with minimum duplication in the analysis.

Table A-4, which is taken from Table B-4 of Reference 1, shows a matrix of the categories of failures in the 120°C stress test. An asterisk indicates that one device from that category was selected for failure analysis. As part of the analysis procedure, the packaged FETs were delidded and SEM photographs were taken of the chip. Figure numbers corresponding to the SEM photographs are given in the right hand column of Tables A-3 and A-4. Observations and comments on the failures follow. The order of presentation is alphabetical by Type Code.

Figure A-11 shows two Type A-51 FETs that exhibited a decrease in drain current. No obvious failure site was found. The close-up view in Figure A-11(b) illustrates the excellent design and fabrication quality of the FET chip. The air-bridge construction details are clearly shown.

The Type D-22 FET shown in Figure A-12 failed during initial placement in the oven. Figure A-12(b) shows that the failure occurred from a gate short circuit.

E3040



(a)



(b)

Figure A-10 Type R-51 #3 FET that had a high resistance source. (a) 240X.
(b) Corroded source lead. 240X.

TABLE A-3
FAILURE ANALYSIS OF PACKAGED DEVICES FROM 120°C CONSTANT STRESS TEST

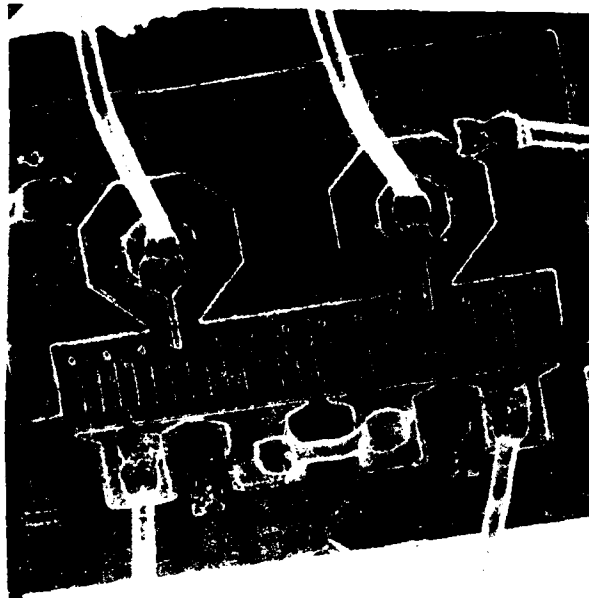
Serial Number	Type Code	Biased/Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Related Failure	Other Failures	Figure Number
1-A	H-21	B	2,439				
1-B	A-51	B		345	I _{DS}		A-11(a)
2-A	H-21	B	2,439				
2-B	R-51	U		345		Set up	
3	H-21	B	2,439				A-14
4-A	H-21	B		345		Set up	
4-B	D-22	B		369	G/S Short		
4-C	R-51	B		345		Set up	
4-D	A-51	B		345	I _{DS}		A-11(b)
5-A	H-21	U	2,439				
5-B	D-22	U		345		Set up	A-12
21	N-21	U		345	I _{DS}		
22	N-21	U		345	I _{DS}		
23	N-21	B		369	G/S Short		A-15
28	N-31	U		2,439		Lost	
33	H-1A1	B	2,439				
34	H-1A1	B		2,439	I _{DSS}		A-13
36	H-1A1	U		345	I _{DS}		
37	H-1A1	U	2,439				
38-A	H-1A1	U		345	I _{DS}		
38-B	N-32	B		96	G/S Short		A-17
39†	N-21	U		345	I _{DS}		A-16
48	N-32	U	2,439				A-18
75	N-31	B		345		Lead	
78	N-31	B	2,439				
79	N-31	U	2,439				

†Note: Device #39 was carried in inventory as a Type N-32 FET. See text.

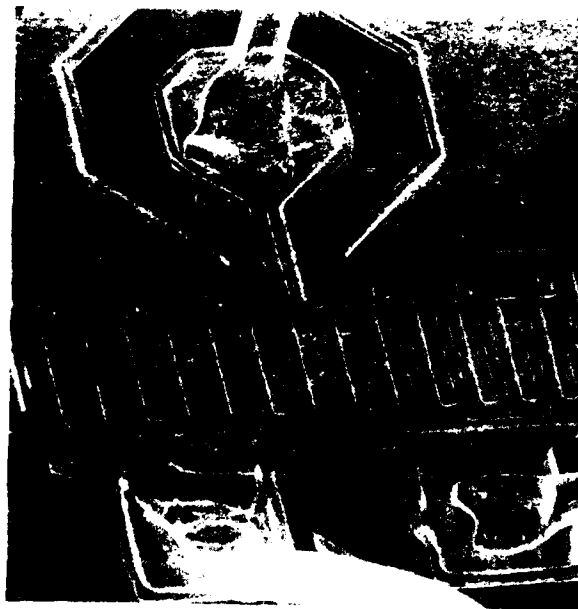
TABLE A-4
CATEGORIES OF FAILURES IN 120°C CONSTANT STRESS
TESTS ON PACKAGED DEVICES

Type Code	No. FETs Started		Not Failed		Set-Up Failures		Related to Temperature						Figure Numbers
							Temper- ature Failures	Gate Control		Gate Short	Open Source	Drain Current	
	B	U	B	U	B	U		B	U				
A-51	2						2					2*	A-11
D-22	1	1		1*			1		1				A-12
H-1A1	2	3	1	1			1	2				1* 2	A-13
H-21	4	1	3*	1	1								A-14
N-21	1	3					1	3		1*		3	A-15, A-16
N-31	2	2	1	1	1	1							A-17, A-18
N-32	1	1		1*			1		1*				
R-51	1	1			1	1							
Totals	14	12	5	4	3	3	6	5	3			3 5	

*Discussed in the text



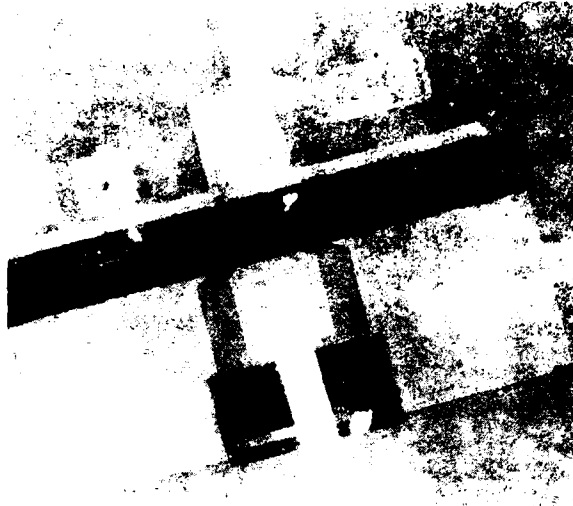
(a)



(b)

Figure A-11 Type A-51 FETs that showed a decrease in drain current.
(a) #1-B at 200X. (b) Left region of #4-D at 600X.

E3042



(a)



(b)

Figure A-12 Type D-22 #5-B FET that failed during set-up. (a) 240X. (b) 1400X.

The SEM photograph of the Type H-1A1 FET shown in Figure A-13(a) is similar in appearance to Figure A-3(b). Voids in the ohmic contact metallization and nodules on the aluminum gate transition are evident. A close-up view of the nodules is shown in Figure A-13(b). Also noteworthy is a ridge in the gallium arsenide.

Figure A-14 gives an overall picture and a close-up view of a biased Type H-21 FET that did not fail with 2,439 hours logged at 120°C. The gate metallization has a ragged edge similar to that shown in Figures A-4(b) and A-5(b).

A gate-to-source short circuit was the failure mode of the Type N-21 FET shown in Figure A-15. The failure occurred in the characteristic location at the gate-pad-to-gate-finger transition.

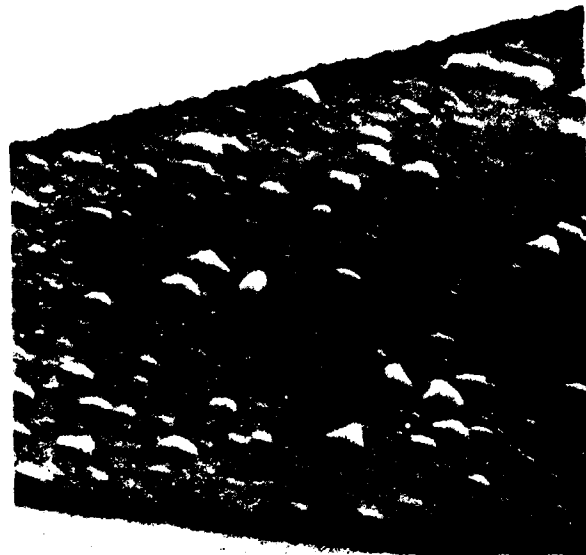
Figure A-16(a) is an overall view of another Type N-21 FET. The melted areas on the gallium arsenide surface apparently occurred during our delidding operation and are not associated with the failure mode of the device. A close-up view of the critical gate-pad-to-finger transition is shown in Figure A-16(b), where minor irregularities in the surface of the aluminum appear. This device has been carried in inventory and throughout our stress testing program as a Type N-32. However, after delidding when we could observe the chip, we saw that the device was Type N-21.

Extensive corrosion was found on the Type N-32 FET, as is evident in Figure A-17. The actual failure was a gate-to-source short circuit. However, it is apparent that the device was prone to failure because of the extensive metallization degradation. The FET failed in 96 hours at 120°C, by a factor of three the shortest time to failure of all 54 devices subjected to the medium temperature stress tests. Failures of this type could be screened out by subjecting all incoming FETs to an initial burn-in period.

Finally, the Type N-32 FET pictured in Figure A-18 indicates deterioration in the gate channel and in the adjacent ohmic contact metallizations. Although officially listed as still within specifications after 2,439 hours of 120°C stress, the device obviously has quite limited value at this point. Figure A-18(b) should be compared with Figure A-9.



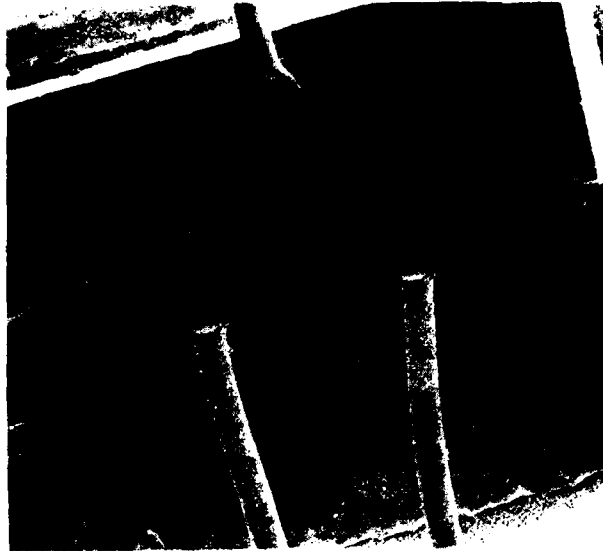
(a)



(b)

Figure A-13 Type H-1A1 #34 FET that showed a decrease in I_{DSS} . (a) 1000X. Note ridge in gallium arsenide and nodules in aluminum. (b) Close-up picture of nodules at 6000X. The view has been rotated 180° from (a).

E 3044



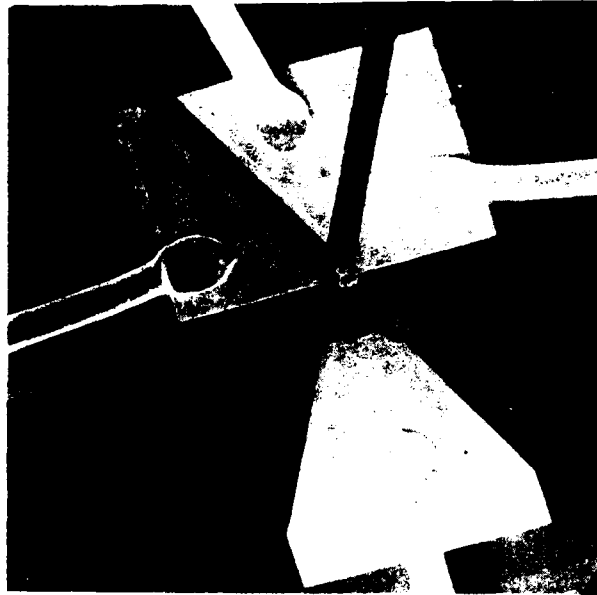
(a)



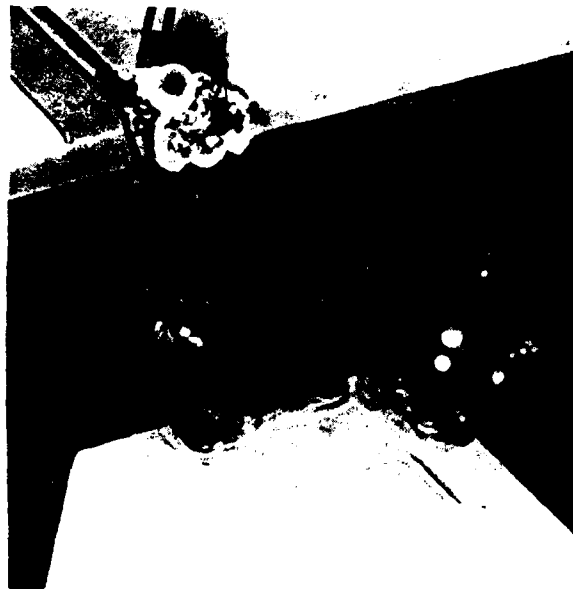
(b)

Figure A-14 Type H-21 #3 FET that did not fail.
(a) 200X. (b) 1820X.

E3045



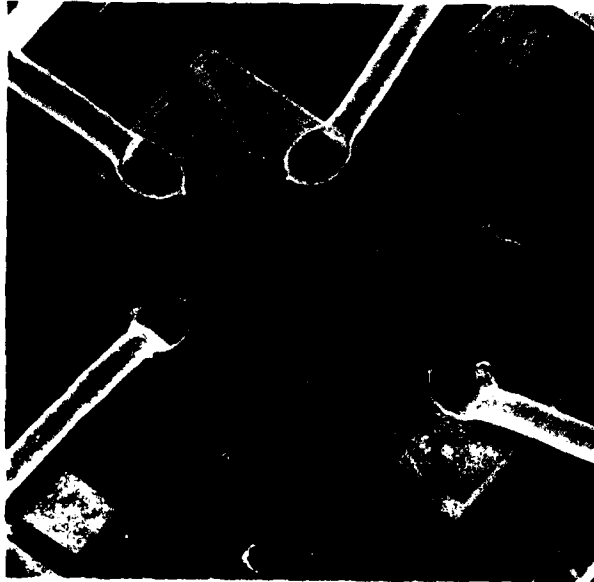
(a)



(b)

Figure A-15 Type N-21 #23 FET with a
gate-to-source short circuit.
(a) 230X. (b) 1800X.

E3046



(a)



(b)

Figure A-16 Type N-21 #39 FET that showed a decrease in drain current.
(a) 200X. (b) 6000X.

E3047



(a)

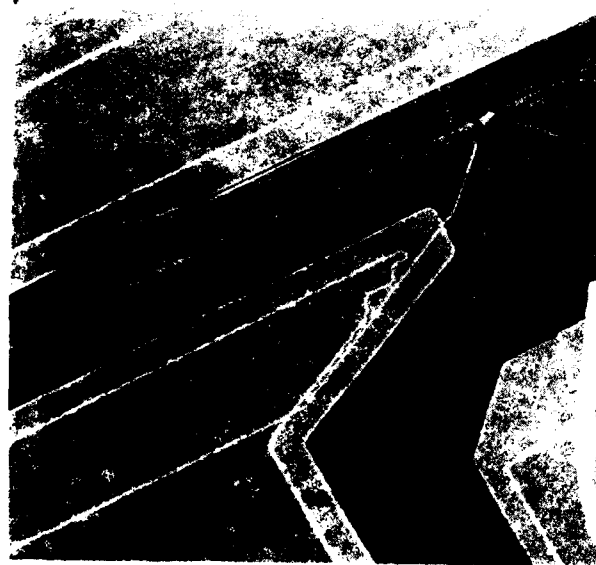


(b)

Figure A-17 Type N-32 #38-B FET that failed
with a gate-to-source short circuit.
(a) 200X. (b) 520X.



(a)



(b)

Figure A-18 Type N-32 #48 FET showing deterioration in the gate channel and adjacent ohmic contact metallizations. (a) 200X. (b) 1820X.

A.1.1.3 Summary of Results of the Medium Temperature Constant Stress Tests - A few general comments can be made about the failure modes of these packaged FETs. First, no distinction was apparent in the device failure modes at 85°C and at 120°C. The failure modes tended to be device-specific, as the Type H-1A1 and Type H-21 FETs had metallization anomalies, and the Type R-51 FETs typically showed source lead corrosion. Biased devices seemed not to fare differently from unbiased devices. Best overall performance was turned in by devices made by manufacturer N. An appropriate burn-in period for the FETs and device screening and qualification procedures tailored to the specific application are necessary for optimum system reliability.

A.1.2 RF Constant Stress Test

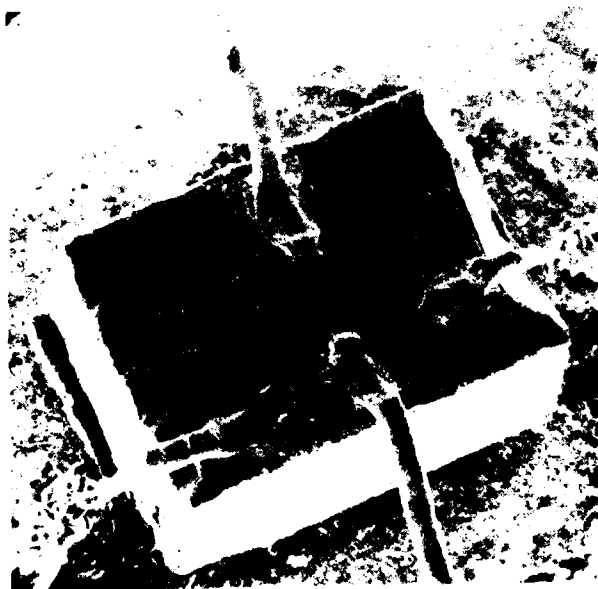
Details of the RF constant stress test are given in the final report of the Reliability Program.⁽¹⁾ In addition to the stress of a 200°C baseplate temperature, the FETs were driven by an RF input signal below the gain saturation point of the FETs operating as amplifiers at 5.7 GHz. Nine devices in all were tested.

A.1.2.1 Type R-51 FET - The RF constant stress test originally had been planned to include packaged Type R-51 FETs. However, after two Type R-51 FETs had been prepared for the RF test, a preliminary check of their RF characteristics indicated anomalous behavior. These two FET packages were delidded and the chips were examined in the SEM. The photographs are shown in Figure A-19. Clearly, the source bond leads have become corroded from the die bond eutectic solder on both the #10 and #20 FETs. In addition, the #20 FET is cracked at the bottom of the die.

The anomalies shown in Figure A-19 are reminiscent of similar difficulties of corrosion and a cracked die that were discovered previously with Type R-51 FETs, as shown in Figures 3-4 and 3-5. A third unmounted, packaged Type R-51 FET that had been planned for the RF stress test was delidded and was also found to have corrosion. As a consequence of these findings, the Type R-51 FETs were deleted from the RF stress plan. Recommendations for screening procedures to cull similar failures before system use are given in Section 3.3.



(a)



(b)

Figure A-19 (a) Type R-51 No. 10 FET showing corrosion of the source bond wires (130X); (b) Type R-51 No. 20 FET showing similar corrosion (150X). Note on the left that the bottom of the die is fractured.

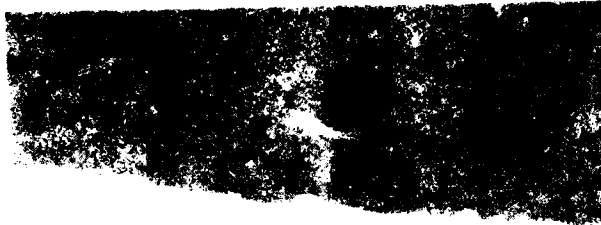
A.1.2.2 Type E-1 FET - The first FET to be placed on the RF stress test was a Type E-1 device, serial number 1R. Details of the test conditions are given in Section 7.3 of Reference 1. This FET logged 1438 hours of operation at 200°C baseplate temperature with -5 dBm RF input power and about 5 dB gain at 5.7 GHz. The RF output power was monitored regularly and changed by less than 0.1 dB over the course of the test. This FET did not fail during the RF constant stress test. Subsequent testing disclosed a leaky gate diode characteristic.

We terminated the test and delidded the package to examine the FET chip. An overall SEM photograph of the failed device is shown in Figure A-20(a). The half-micron gate stripe is ragged with sharp, irregular aluminum edges on a microscopic scale. The gate is offset toward the source metallization. Near one gate pad connector, one arm of the gate stripe appears to lack full aluminum coverage. At this same location the gate stripe is bridged to the grounded source pad. Figure A-20(b) shows a close-up SEM photograph of these observations. Farther along the gate stripe, near the other gate pad connector, the gate metallization is mounded by what appears to be incomplete etching of the gate channel.

Apparent also are the numerous voids in the gold metallization of the source and drain ohmic contacts. EDAX scans have verified that gold has largely disappeared from the void areas, but that it has not migrated to the gate.

From a companion lot three similar packaged devices that had not been subjected to formal temperature or electrical stress tests were DC characterized. These were all found to exhibit DC failures of a poor Schottky-barrier diode characteristic and excessive gate currents. SEM examination of the FET chips showed the same type of physical gate problems at approximately the same relative topographic locations on the gate stripe as the stressed FET showed. Voids were also observed in the ohmic contact gold metallization, but to a much lesser extent than on the stressed Type E-1 FET #1R. It therefore appears likely that the FETs were prone to failure and that the processing, mounting, and bonding operations and DC testing procedures merely precipitated the actual failures on some devices.

E3005



(a)



(b)

Figure A-20 (a) SEM photograph of the Type E-1 #1R FET at 400X; (b) Close-up SEM photograph of the gate connector region at 3360X.

Thus, it appears that the gold contact metallization voids and also the raggedness of the gate result from non-optimum processing procedures. As explained in Appendix B of Reference 1, this type device was deleted from the test plan, so that no additional devices of this type were analyzed.

As no Type E-1 FETs were available for the earlier temperature stress tests, we lack comparison data on failure modes. However, we have no indication that the applied RF power had any noticeable effect on the failure modes of this type FET. Improved reliability of this type device depends on improvements in device processing.

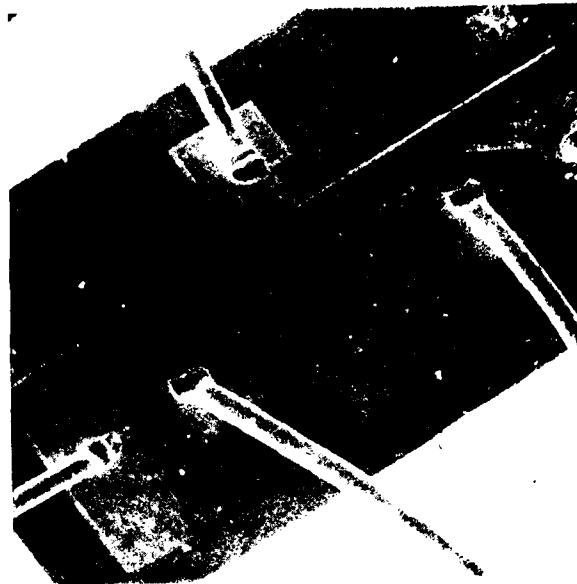
A.1.2.3 Type D-11 FET - The next FET to be placed on the RF stress test was a type D-11 device, serial number 2R. Test conditions were similar to those for the Type E-1 FET. The device logged 1087 hours of operation at 200°C baseplate temperature with -10 dBm RF input power and about 6.5 dB gain at 5.7 GHz. The RF gain was monitored regularly and changed by not more than 0.4 dB over the course of the test. This FET did not fail during the RF constant stress test. Subsequent measurements showed a leaky gate diode characteristic and excessive pinch-off voltage.

We terminated the test and delidded the package to examine the FET chip. Figure A-21(a) shows an overall SEM photograph of the failed device. Figure A-21(b) shows a magnified view of the left gate connector. Slight mottling of the source and drain ohmic contact metallizations is evident. The gate transition is imperfectly formed. However, it was not apparent that this construction defect affected either the DC measurements or RF performance. The gate metal is gold, and the gate width is nominally one micrometer.

A.1.2.4 Other FETs from RF Constant Stress Test - Table A-5, identical with Table B-5 of Reference 1, shows the status of the FETs when the RF stress test was terminated. The first two FETs listed, the #1R and #2R devices, have already been discussed. Of the remaining seven FETs, three failed because of excessive changes in DC drain current. Four FETs did not fail. None of the FETs in the RF stress test showed more than 1 dB decrease in RF gain during the course of the tests.

No effects directly ascribable to the applied RF power were found. The baseplate temperature of 200°C was therefore the stress agent. No device failed

E-3049



(a)



(b)

Figure A-21 (a) SEM photograph of the Type D-11 #2R FET at 200X; (b) Close-up of the left gate connector region at 3000X.

TABLE A-5
STATUS OF PACKAGED DEVICES WHEN THE
200°C RF STRESS TEST WAS TERMINATED

Serial Number	Type Code	Not Failed, Hours	Hours to Failure	RF Gain, dB		Failure Mode	Figure Number
				Initial	Final		
1R	E-1		1438	5.4	5.4	Leaky gate	A-20
2R	D-11		1087	6.8	6.4	Leaky gate	A-21
3R	H-1A1		477	3.6	2.9	ΔI_{DS} , ΔI_{DSS}	
4R	H-1A1	477		1.8	1.2		
5R	H-1A1	477		2.0	1.3		
6R	D-11		477	4.0	3.5	ΔI_{DS} , ΔI_{DSS}	
7R	D-11		477	4.6	4.6	ΔI_{DS} , ΔI_{DSS}	
8R	N-32	452		4.0	4.0		
9R	N-32	452		4.0	4.0		

catastrophically. Neither of the two Type N-32 FETs failed, nor showed any degradation in RF gain.

Of the three Type H-1A1 FETs, only one failed, and that failure was due to a change in drain current. This type of temperature-induced failure mode has already been discussed adequately, and SEM photographs of two such failed FET chips were presented in Figures A-3 and A-13.

The remaining two devices, Type D-11, failed by an excessive change in drain current. Temperature-induced failures of Type D-11 FETs (Type D-1 chip) have been discussed previously. SEM photographs are shown in Figures 3-14, 3-15, A-2 and A-21. Mottling of the gold gate metallization is the predominant degradation-type feature of these devices.

Our expectation, based on these considerations, was that no new information on failure modes would be developed from destructively analyzing any of the remaining seven FETs in Table A-5. Consequently, these FETs were retained intact and are available for later work.

The Type N-32 FETs performed best, followed by the Type H-1A1 FETs. These conclusions are consistent with our previous findings concerning reliability of FETs made by manufacturer N and by manufacturer H. We again caution that results reported here were obtained using transistors at least two years old. We suggest for present system needs that devices of recent manufacture from several vendors be evaluated.

A.2 RADC/TI MEDIUM POWER FET RELIABILITY PROGRAM

A number of failed devices from the RADC/TI program were analyzed in Section 4. We received thirty-six additional failed devices from RADC, along with data sheets describing the stress tests and the observations of failure at TI. We selected devices exhibiting typical failures and examined them in the SEM. Table A-6 lists details of the stress tests and observations of failure at TI. The type code "T-LAB" refers to laboratory devices that may vary in fabrication. "Test Type" refers to the categories

TABLE A-6
OBSERVATIONS OF FAILURES OF
STRESSED MEDIUM POWER GaAs FETs RECEIVED FROM RADC

<u>Type Code</u>	<u>Number</u>	<u>Test Type</u>	<u>Detail of Stress Test</u>	<u>Observation at TI</u>	<u>Figure Number</u>
T-LAB	1	A	Drain bias increased until failure with zero gate voltage	Failed catastrophically at 23V	
T-LAB	2	A	Drain bias increased until failure with zero gate voltage	Failed catastrophically at 21V	
D-250/6	51	A	Drain bias increased until failure with gate pulsed	Failed catastrophically at 19V	22(a)
M-400/6	17J	A	Drain bias increased until failure with gate pulsed	Failed catastrophically at 18V	22(b)
N-300/7	2J	A	Drain bias increased until failure with gate pulsed	Failed catastrophically at 24V	23
T-LAB	17	A	Drain bias increased until failure with gate pulsed	Failed catastrophically at 18V	24(a)
T-X500/8	13J	A	Drain bias increased until failure with gate pulsed	Failed catastrophically at 22V	24(b)
D-250/6	42	A	Drain bias increased until failure with gate and RF pulsed	Failed catastrophically at 8V	
M-400/6	18J	A	Drain bias increased until failure with gate and RF pulsed	Failed catastrophically at 27V	

TABLE A-6
OBSERVATIONS OF FAILURES OF
STRESSED MEDIUM POWER GaAs FETs RECEIVED FROM RADC
(continued)

<u>Type Code</u>	<u>Number</u>	<u>Test Type</u>	<u>Detail of Stress Test</u>	<u>Observation at TI</u>	<u>Figure Number</u>
N-300/7	G43-2-2#25	A	Drain bias increased until failure with gate and RF pulsed	Failed catastrophically at 33V	
T-LAB	18	A	Drain bias increased until failure with gate and RF pulsed	Failed catastrophically at 13V	
T-X500/8	14J	A	Drain bias increased until failure with gate and RF pulsed	Failed catastrophically at 18V	
T-LAB	5	B	Reverse gate bias increased until failure	Failed catastrophically at 25V (140 mA)	
T-LAB	6	B	Reverse gate bias increased until failure	Failed catastrophically at 27V (140 mA) ^e	25
T-LAB	7	C	Forward gate current increased until failure	Failed catastrophically at 1000 mA (2.05V)	26
T-LAB	8	C	Forward gate current increased until failure	Failed catastrophically at 1000 mA (2.02V)	
T-LAB	3	D	Drain bias increased until failure with $V_G = -1.3V$, $P_{in} = 26$ dBm	Failed catastrophically at 19V	27

TABLE A-6
OBSERVATIONS OF FAILURES OF
STRESSED MEDIUM POWER GaAs FETs RECEIVED FROM RADC
(continued)

<u>Type Code</u>	<u>Number</u>	<u>Test Type</u>	<u>Detail of Stress Test</u>	<u>Observation at TI</u>	<u>Figure Number</u>
T-LAB	4	D	Drain bias increased until failure with $V_G = -1V$, $P_{in} = 24.4 \text{ dBm}$	Failed catastrophically at 17V	28
T-LAB	9	E	RF input increased until failure with normal bias	Failed catastrophically at 4.0W	
T-LAB	11	E	RF input increased until failure with normal bias	Failed catastrophically at 5.0W	
D-250/6	36		200°C heat sink, 8V drain bias, $P_{in} = 100 \text{ mW}$	P_{out} decreased 1 dB in 426 hours; device failed afterward during examination of I-V characteristic	
D-250/6	41		200°C heat sink, 8V drain bias, $P_{in} = 100 \text{ mW}$	Failed catastrophically at 228 hours	29
D-250/6	50		200°C heat sink, 8V drain bias, $P_{in} = 100 \text{ mW}$	P_{out} decreased 1 dB in 350 hours	
T-X500/8	16J		200°C heat sink, 8V drain bias, $P_{in} = 100 \text{ mW}$	P_{out} decreased 1 dB after 620 hours	
T-X500/8	18J		200°C heat sink, 8V drain bias, $P_{in} = 100 \text{ mW}$	P_{out} decreased 1 dB after 620 hours	

TABLE A-6
OBSERVATIONS OF FAILURES OF
STRESSED MEDIUM POWER GaAs FETs RECEIVED FROM RADIC
(continued)

<u>Type Code</u>	<u>Number</u>	<u>Test Type</u>	<u>Detail of Stress Test</u>	<u>Observation at TI</u>	<u>Figure Number</u>
D-250/6	24		300°C 325-hour temperature - only stress test	IDS decreased from 615 to 570 mA	
D-250/6	55		300°C 325-hour temperature - only stress test	IDS decreased from 400 to 365 mA	
M-400/6	18		300°C 325-hour temperature - only stress test	IDS decreased from 323 to 285 mA	
N-300/7	G45-2#18		300°C 325-hour temperature - only stress test	IDS decreased from 396 to 340 mA	
N-300/7	G43-2-2#40		300°C 325-hour temperature - only stress test	IDS decreased from 400 to 310 mA	
T-X500/8	18		300°C 325-hour temperature - only stress test	IDS decreased from 307 to 250 mA	
T-X500/8	19		300°C 325-hour temperature - only stress test	IDS decreased from 460 to 415 mA	
D-250/6	25		350°C 236-hour temperature - only stress test	IDS decreased from 575 to 475 mA; device failed while being probed after stress	30

TABLE A-6
OBSERVATIONS OF FAILURES OF
STRESSED MEDIUM POWER GaAs FETs RECEIVED FROM RADC
(continued)

<u>Type Code</u>	<u>Number</u>	<u>Test Type</u>	<u>Detail of Stress Test</u>	<u>Observation at TI</u>	<u>Figure Number</u>
M-400/6	20		350°C 236-hour temperature - only stress test	IDSS decreased from 370 to 230 mA; device failed while being probed after stress	
N-300/7	86M-65#15		350°C 236-hour temperature - only stress test	I-V characteristic became non-ohmic	
T-X500/8	21		350°C 236-hour temperature - only stress test	IDSS decreased from 465 to 212 mA	

of maximum electrical stresses defined in Section 4.2. Where SEM photographs are presented, the figure number is given.

A number of device type codes in Table A-6 can be found in the lists of manufacturer's published specifications presented in Table 2-2. Reports from the RADC/TI program should be consulted for specific information on all device types used in that program.⁽²⁾

A.2.1 Maximum Electrical Limits

This section discusses our observations on devices that were stressed electrically until failure. The order of presentation parallels that of Section 4.2.2. The narrative is keyed to Table A-6.

MAXIMUM DRAIN VOLTAGE (TEST A)

We examined in the SEM eight representative failures of the twelve devices that were subjected to maximum drain bias voltage with various conditions on the gate voltage and RF input power. The failure mode of device Type T-LAB No. 2 with zero gate voltage is similar in appearance to that shown in Figure 4-1 with a relatively small failure site. When the gate was pulsed, the failure tended to be massive, involving all three electrodes, as we observed on Devices D-250/6 No. 42 and No. 51, which is shown Figure A-22(a). Substantially all the FETs show evidence of fusion. That a large drain current was present is evidenced by the fact that three of the four drain wires vaporized.

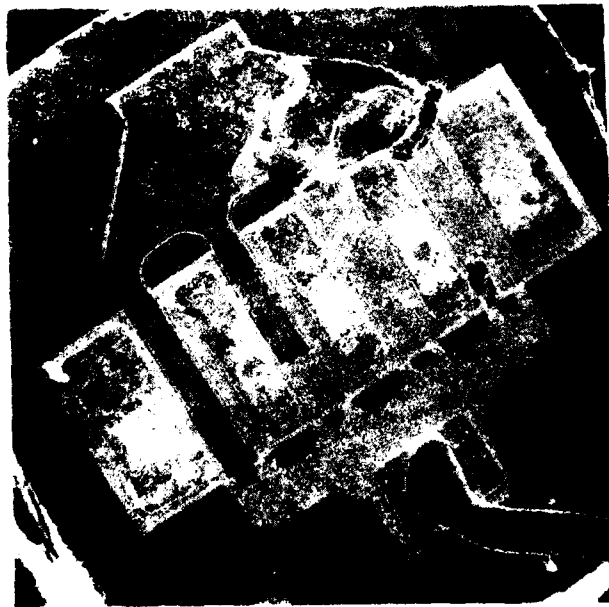
Device Type M-400/6 No. 17J, shown in Figure A-22(b), has two fused regions. Of interest also, is peeling of the drain metallization from most of the left half of the chip.

Two type N-300/7 devices were examined and photographed in the SEM, the No. 2J and No. G43-2-2 #25. The No. 2J FET is shown in Figure A-23. This FET showed the least extensive destruction of all devices that were deliberately failed electrically in Test A. Figure A-23(a) shows that two complete FETs were fabricated in a unit cell,

E3006



(a)



(b)

Figure A-22 Test A failures. (a) Type D-250/6 No. 51 FFT at 156X.
(b) Type M-400/6 No. 17J FET at 214X.

E3007



(a)



(b)

Figure A-23 Test A failure of Type
N-300/7 No. 2J FET.
(a) 100X. (b) 400X.

but that only one was used. Note the substantial source grounding strap in the lower part of the photograph. The excellent quality of this device in fabrication and bonding is clearly evident. Figure A-23(b) shows a close-up view of the failure site. The drain has fused through the gate to the source. The source finger has then fused open where it bridges over the gate feed. Evidently, the source finger at the gate crossover acted precisely as a fuse to interrupt the short circuit current and prevent further destruction of the device.

Figure A-24(a) shows a failed laboratory device, the Type T-LAB No. 17. Interesting construction features are the source grounding strips flanking both sides of the chip and the source grounding blanket across the entire center of the device. Some wicking of the die attach solder on the source leads is evident to the right of the chip. The gate is triple bonded. Mechanical damage is evident, and the drain lead has been scraped off. We made no attempt at removing the source cover to expose the heart of the device, as it was felt that the main effect of this effort would be further mechanical damage to the FET. Therefore, the extent of the electrical failure could not be observed. Figure A-24(b) shows the Type T-X500/8 No. 13J FET. Cratering is apparent near the left drain pad. The left drain lead has melted open.

MAXIMUM REVERSE GATE VOLTAGE (TEST B)

Device Type T-LAB No. 6 was selected for examination. An overall SEM photograph is shown in Figure A-25(a). Note that this laboratory device differs considerably in appearance from the laboratory device T-LAB No. 17 in Figure A-24. The failure occurred at the gate pad-to-finger junction, shown in the lower left region of the photograph, and involved the source and drain as well. A close-up view of the failure site is shown in Figure A-25(b), which shows the localized melting that occurred.

MAXIMUM FORWARD GATE CURRENT (TEST C)

In this test the forward gate current was increased until the device failed. Figure A-26(a) shows an overall SEM photograph of the Type T-LAB No. 7 FET. Note that this device differs in overall appearance from both the previous T-LAB devices shown in Figures A-24 and A-25. Failure occurred at 1000 mA by fusion of both ends of the

E3008



(a)



(b)

Figure A-24 Test A failures. (a) Type T-LAB No. 17 FET at 250X.
(b) Type T-X500/8 No. 13J FET at 250X.

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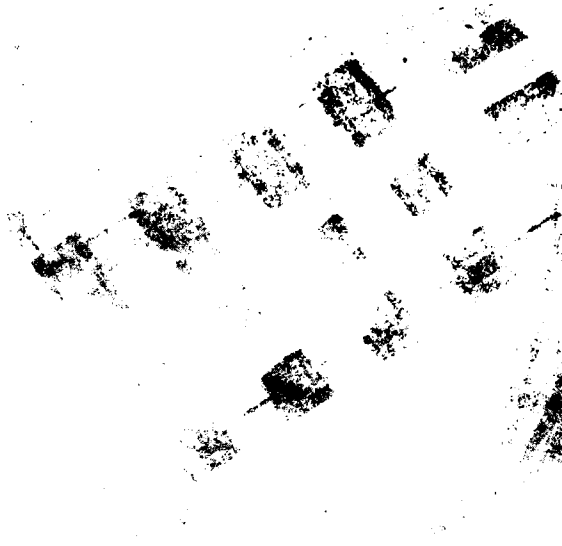
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(a)



(b)

Figure A-25 Test B failure of Type
T-LAB No. 6 FET. (a) 200X.
(b) 2550X.

second drain finger from the left with adjacent gate stripes and source pads. Considerable debris arising from opening the package is evident. No cleaning of the chip was attempted in order to preserve the delicate failure nodules on the side of the gate stripe. These appear near the gate contact end of the gate stripe close to a failure site. A close-up view of the nodules is shown in Figure A-26(b). The small size of the nodules precluded EDAX investigation of their composition.

MAXIMUM DRAIN VOLTAGE UNDER OPERATING CONDITIONS (TEST D)

The failed Type T-LAB No. 3 FET is shown in Figure A-27. The failure site is small and is similar in appearance to that of the Type T-LAB No. 2 FET of Test A. In both Test A and Test D the drain bias was increased until failure with constant gate bias. For Test A the gate bias was set at zero volts, and no RF was applied. For Test D the gate bias was set at the operating level of -1.3 volts, and an RF input power level of + 26 dBm was present. Our observation for maximum applied drain voltage is that for constant gate voltage the failure site is small, and for pulsed gate voltage the failure is extensive, whether normal levels of RF power are applied or not.

MAXIMUM CW RF INPUT POWER (TEST E)

In this test the DC bias was normal, and the RF input power was increased until failure occurred. Based on TI's test results for two Type T-LAB FETs, the RF CW input power burnout level is between four and five watts. As was true with other types of devices (see page 90), the failure on the Type T-LAB No. 9 FET occurred at the gate pad to gate finger junction. The failure was a "flashover" type between the gate and the grounded source. SEM photographs of the device are shown in Figure A-28.

A.2.2 Temperature Stress Tests

A stress test was carried out at TI on three type D-250/6 FETs and on two Type T-X500/8 FETs at 200°C heat sink temperature with 8 V drain bias and an RF input power of 100 mW. A decrease in RF output power of 1 dB or more constituted failure. All five devices listed in Table A-6 were examined in the SEM. Typically, SEM photographs of these degradation type failures leave nothing unusual to observe, with the possible exception of minor irregularities in the glass passivation layer.

E3010



(a)



(b)

Figure A-26 Test C failure of Type
T-LAB No. 7 FET. (a) 225X.
(b) 3000X.

E3011

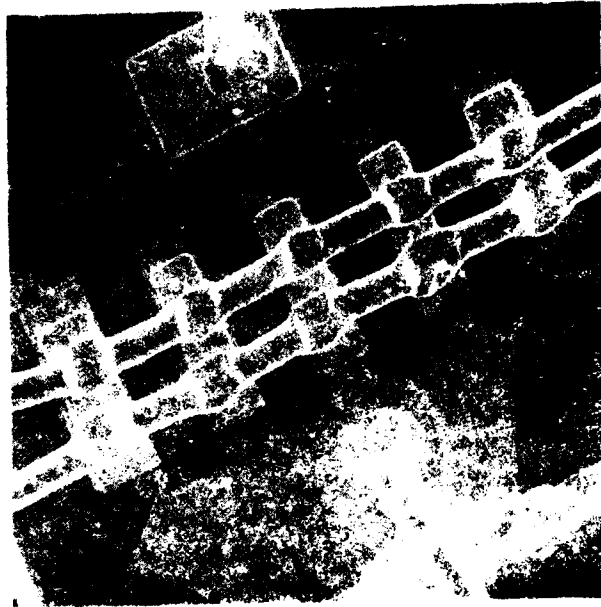


Figure A-27 Test D failure of Type T-LAB
No. 3 FET at 180X.

E3012



(a)



(b)

Figure A-28 Test E failure of Type
T-LAB No. 9 FET. (a) 180X.
(b) 1500X.

E3013



(a)



(b)

Figure A-29 Catastrophic failure of Type D-250/6 No. 41 FET at 228 hours of 200°C heatsink temperature, 8V drain bias, $P_{in} = 100$ mW. (a) 144X. (b) 2800X.

Device Type D-250/6 No. 41 did fail this test catastrophically at 228 hours. SEM photographs of the FET are shown in Figure A-29. The failure occurred between the gate-pad-to-gate-finger junction and the grounded source. The similarities between Figure A-29 and Figure 4-16 should be noted. Also visible in Figure A-29(b) is a dark region on the drain ohmic contact, similar to that shown in Figure 4-20(b). A discussion of such defects on Type D-250/6 FETs is given on page 108.

Another series of temperature-only stress tests was carried out at TI at 300°C for 325 hours on seven devices, as is detailed in Table A-6. The failures all were degradation in I_{DSS} . Two FETs of this series were examined, the Type D-250/6 No. 55 and the Type T-X500/8 No. 19. No evidence of failure was observed in either device.

Finally, four FETs were given a temperature-only stress test at 350°C for 236 hours. All four of these devices were photographed in the SEM. The Type D-250/6 No. 25 failed while being probed after the stress test. An overall SEM photograph of the FET is shown in Figure A-30(a). The large short-circuit current melted a drain lead and two source wires. A failure site can be observed at the gate-pad-to-gate-finger junction involving all three electrodes. A close-up view is shown in Figure A-30(b). This failure involves the drain also, but otherwise is quite similar in appearance to those shown in Figures 4-16(b) and A-29(b). Some degradation in the gold metallization can also be observed in Figure A-30(b).

The Type M-400/6 No. 25 device sustained considerable mechanical damage that tends to obscure the electrical failure. A close-up view disclosed limited voiding in the gold gate pad metallization. No failure site was observed in the Type N-300/7 No. 86M-65#15 FET. On the Type T-X500/8 No. 21 FET a slight surface defect was observed in the glass passivation layer.

E3014

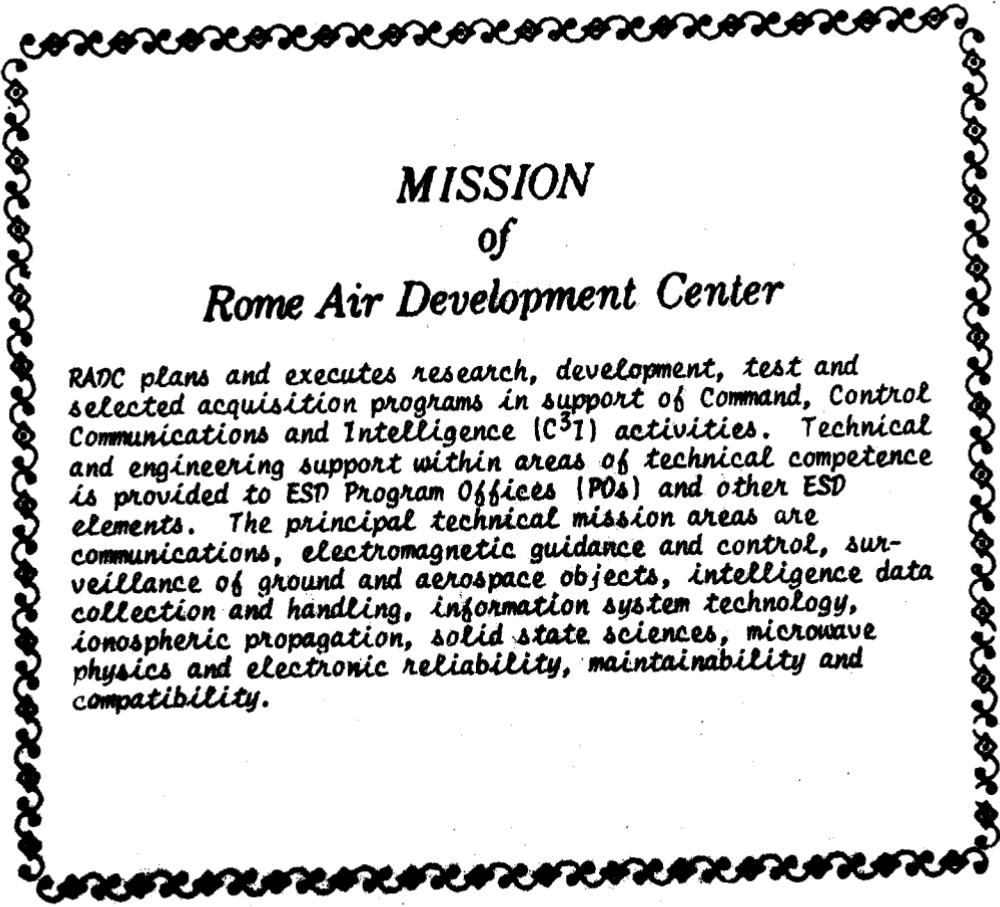


(a)



(b)

Figure A-30 Failed Type D-250/6 No. 25 FET after
236 hours at 350°C. (a) 150X.
(b) 2100X.



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